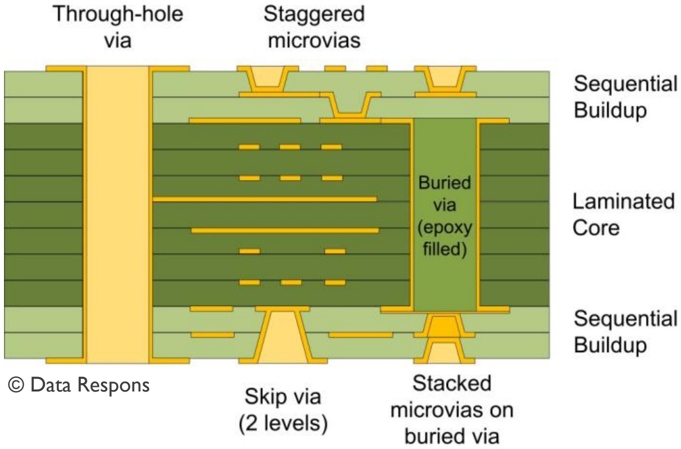
HIGH-DENSITY INTERCONNECT PCB TECHNOLOGY FOR SPACE APPLICATIONS

M. CAUWE – 23/10/25 – ELECTRONIC COAST SEMINAR

HDI PCB TECHNOLOGY FOR SPACE APPLICATIONS

INTRODUCTION

- Large ASICs (Application Specific Integrated Circuits) and FPGA (Field Programmable Gate Arrays) are now commonly used on-board spacecraft
- New generation FPGAs (Virtex-5QV from Xilinx) have pin count above 1000 pins, with an interconnect pitch reduced to 1.0 mm
- Fan-out routing for these packages requires high-density interconnect (HDI) PCBs using microvias and fine lines



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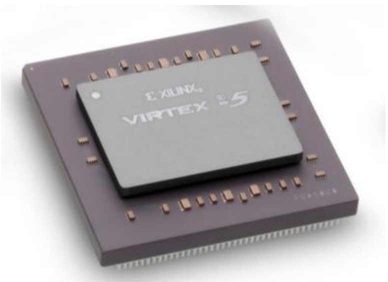
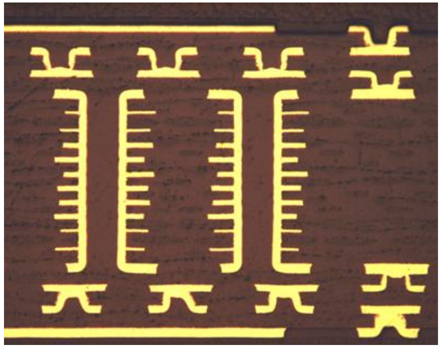


NASA - NEPP



ACB

HDI PCB TECHNOLOGY FOR SPACE APPLICATIONS

DEVELOPMENT ROADMAP

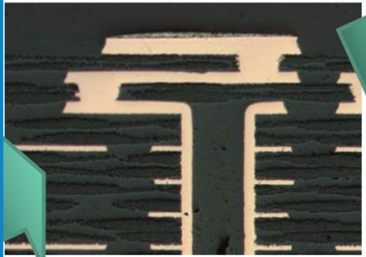
Complexity

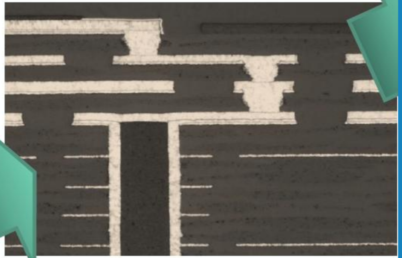
1 mm pitch CGA
1752 I/Os
V5, RTG4

0.8 mm pitch COTS
CBGA 323
PBGA ~3000 I/Os

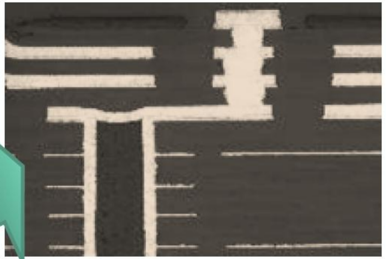
Single uvias
Polyimide
SnPb

Staggered uvias





Semi-stacked uvias
High speed dielectric
Backdrilling on core vias
ENIG and solder mask



3 stacked uvias
Spread glass weave
Smooth copper foil
Ni-free finish

ECSS-Q-ST-70-12C
Not Qualified

6.25 Gbps

HDIPCB project objectives:
Qualify, Verify, Evaluate & Investigate

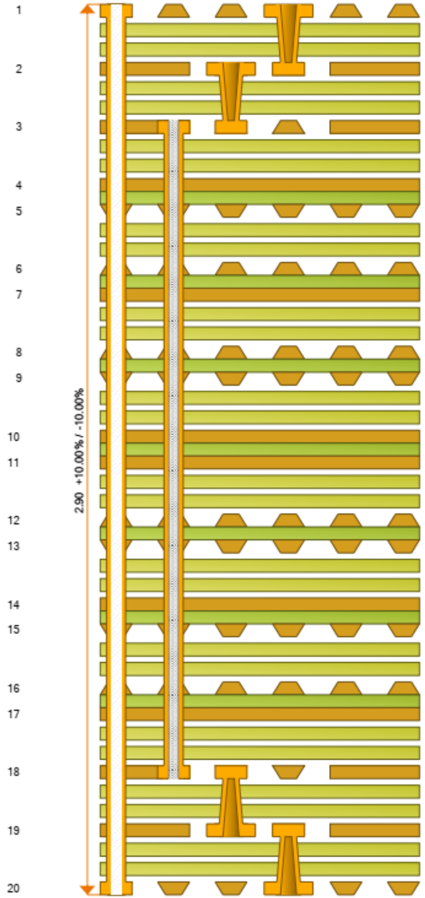
28 Gbps

Data rate

HDI PCB TECHNOLOGY FOR SPACE APPLICATIONS

BASIC HDI TECHNOLOGY

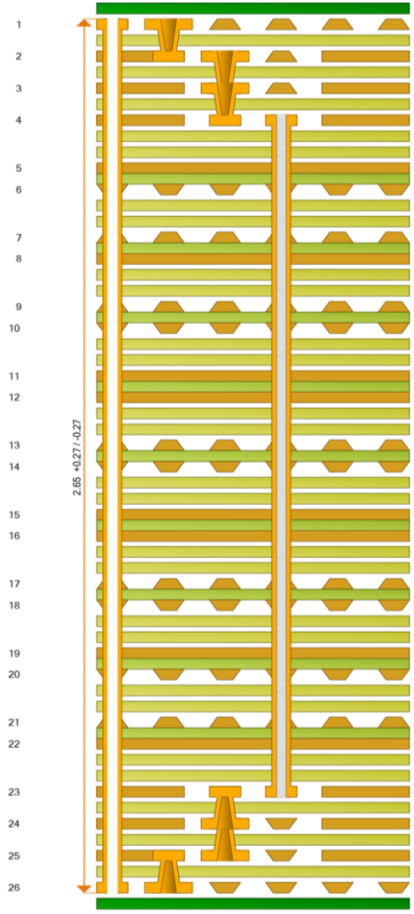
Technology parameter	Basic HDI
Conductor width and spacing	70/70 µm (no plating, 17 µm Cu foil)
Configuration of microvias	2 levels staggered, copper filled, 175 µm diameter
Number of layers	≤ 20
Construction of HDI layers	Microvias staggered to core, two sheets of prepreg
Aspect ration of core vias	≤ 7
PCB thickness	2.8 mm
Filling medium for core vias	Via plugging paste (+ cap plating)
Construction of core	Single sequence
Dielectric material	Polyimide (Ventec VT-901)
Surface finish and solder mask	SnPb, no SM



HDI PCB TECHNOLOGY FOR SPACE APPLICATIONS

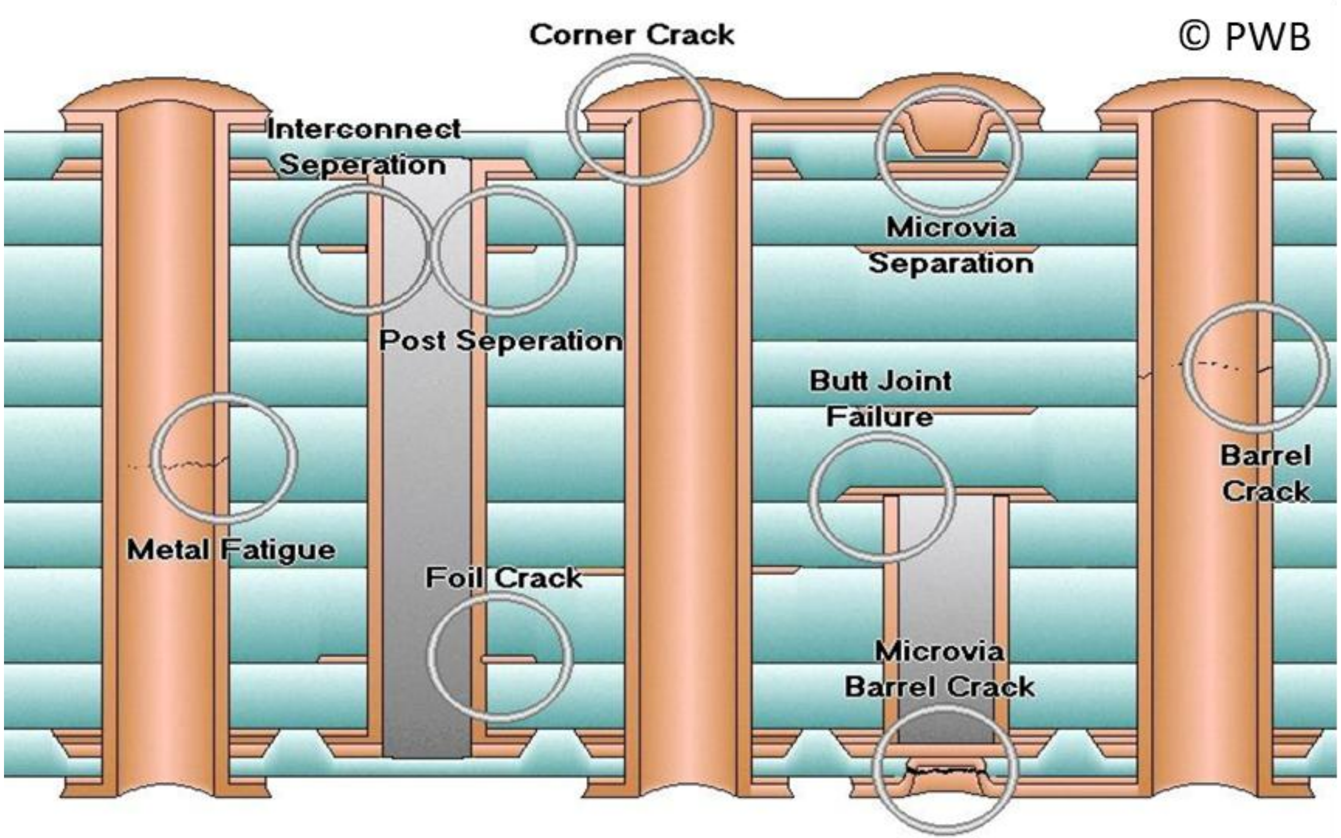
COMPLEX HDI TECHNOLOGY

Technology parameter	Complex HDI
Conductor width and spacing	50/50 µm (no plating, 12 µm Cu foil)
Configuration of microvias	3 levels, Cu fill, 125 µm diameter Semi-stacked configuration
Number of layers	≤ 26
Construction of HDI layers	Staggered, one sheet of prepreg
Aspect ration of core vias	≤ 10
Filling medium for core vias	Via plugging paste (+ cap plating)
Construction of core	Single sequence
Presence of non-functional pads	Full pad stack removed
Back drilling	Buried vias
Dielectric material	Ventec VT-901 and Megtron 6
Surface finish and solder mask	ENIG or ENEPIG with solder mask



HDI PCB TECHNOLOGY FOR SPACE APPLICATIONS

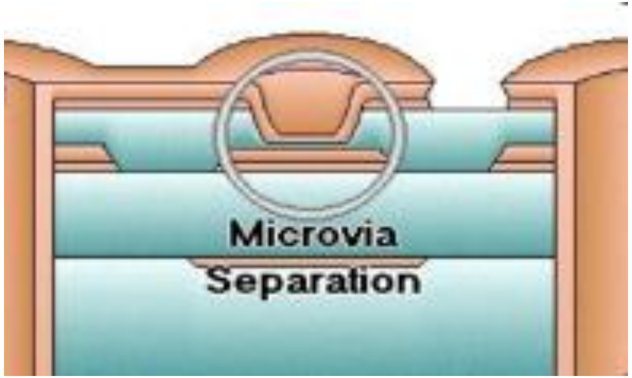
HIERARCHY OF FAILURE FOR HDI TECHNOLOGY

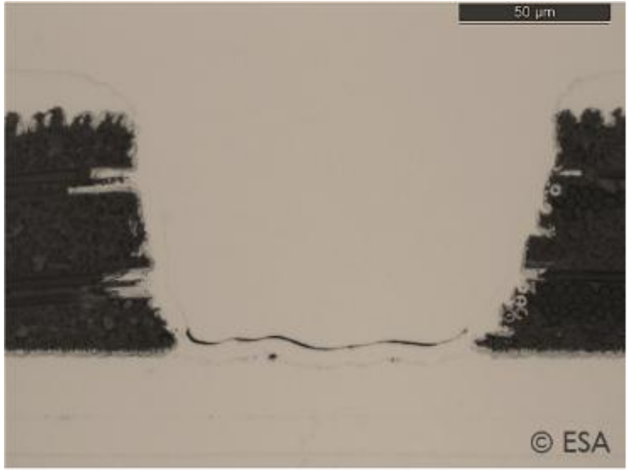


LESSONS LEARNT ON MICROVIAS

A HIDDEN RELIABILITY THREAT

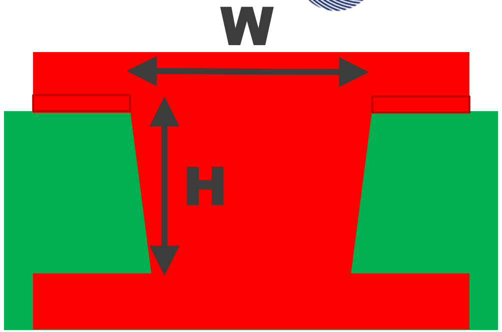
- Microvias can fail for the following reasons:
  1. Non-optimised materials or processes
  2. Stressful design
  3. Inhomogeneous processes
- Weakness in microvia target land interface is not caused by any single manufacturing process
- ESA evaluates microvia designs using
  a. review of design and comparison to qualification
  b. thermo-mechanical modelling
  c. testing coupons and spare PCBs
  d. review of manufacturing processes





LESSONS LEARNT ON MICROVIAS

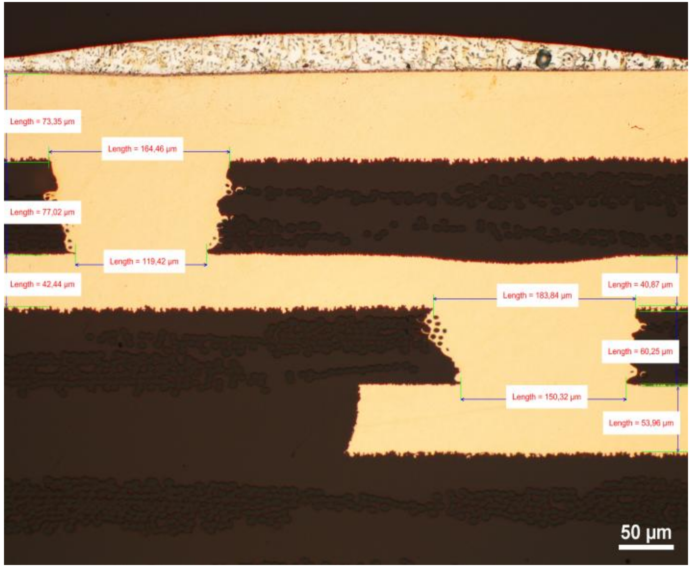
REVIEW OF DESIGN AND MANUFACTURING PROCESSES



- ESA microvia process guidelines: [ESA-TECMSP-TN-19672]
- Aspect ratio of 0.66 to 0.75 advised for high-quality microvias
- Dielectric thickness is important contributor to aspect ratio

- Design recommendations
  - Use the microvia layers as plane layers (max Cu area)
  - Select prepreg construction for worst-case Cu thickness
  - Stagger multiple levels of microvias (tangency of pads)

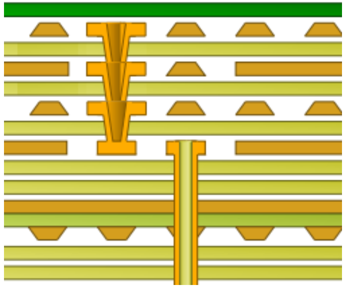
- Manufacturing recommendation
  - Minimize copper thickness on microvia layers



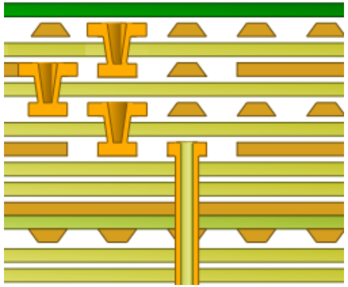
LESSONS LEARNT ON MICROVIAS

FROM TWO TO THREE LEVELS OF MICROVIAS

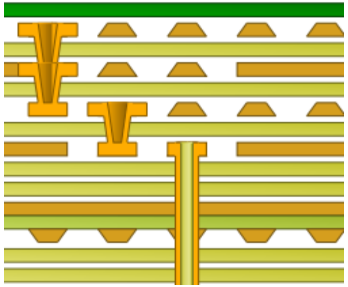
- Three levels of microvias allow optimal power integrity while still offering a high routing density on the buildup layers
- A balance between design, manufacturability and reliability needs to be found



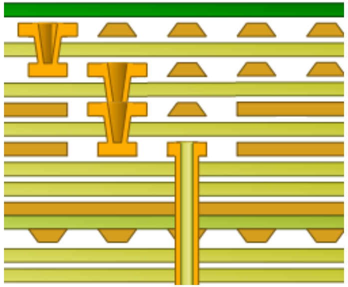
FULL STACKED



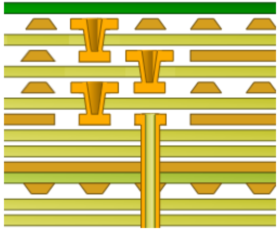
FULL STAGGERED



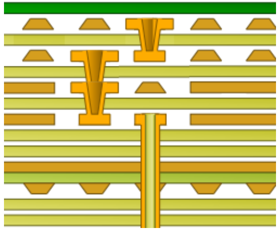
SEMI-STACKED OUTSIDE



SEMI-STACKED INSIDE



STAGGERED ABOVE BV

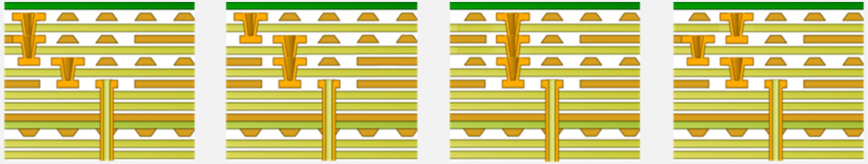


SSI ABOVE BV

LESSONS LEARNT ON MICROVIAS

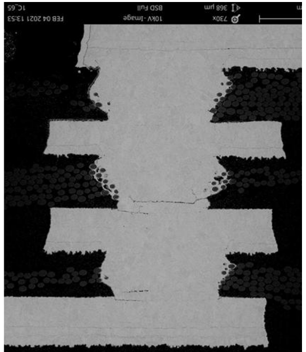
THREE LEVELS OF MICROVIAS – TEST RESULTS

- When manufacturing quality is high, microvias will not reduce the reliability of the HDI PCB
- Robustness testing at elevated temperatures can differentiate between microvia configurations (robustness ≠ reliability)
- Results for all test methods were consistent

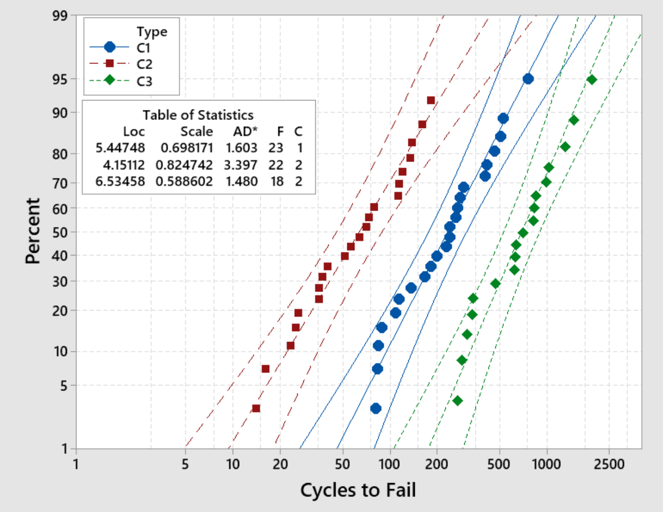


	SEMI-STACKED OUTSIDE			SEMI-STACKED INSIDE			FULL STACKED			FULL STAGGERED		
	FR4	PI	RF	FR4	PI	RF	FR4	PI	RF	FR4	PI	RF
2.6.27B (REFLOW)	++	++	++	++	++	++	++	--	-	++	++	++
2.6.7.2C (CYCLING)	+	+	+	+	+	+	-	-	-	++	++	++
2.6.26A (CITC)				++	+	+	+	+	-	++	++	++
2.6.26A (IST)	++			++	+	+	+			++		

CITC – 283 cycles to 230 °C



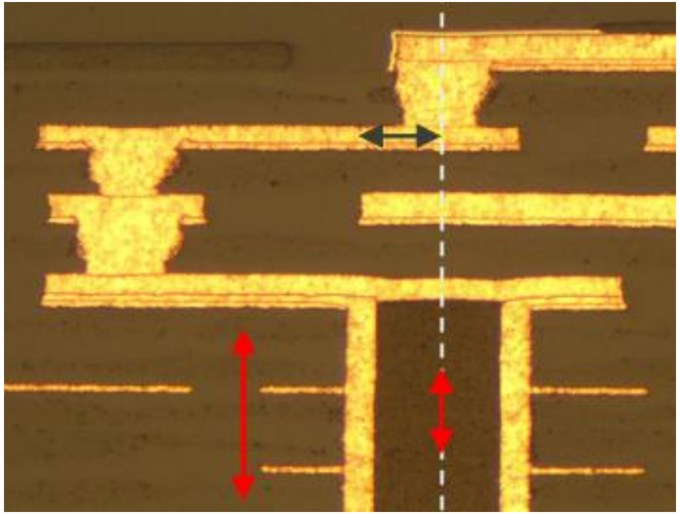
IST – 4272 cycles to 190 C

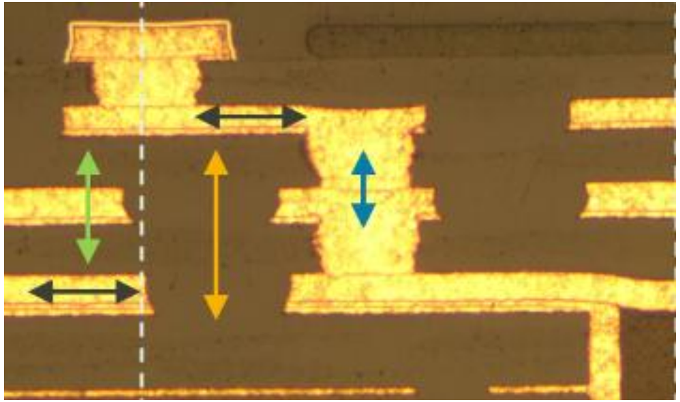


LESSONS LEARNT ON MICROVIAS

DESIGN RECOMMENDATIONS

- Distance between microvia stack and core via should be maximized (design rule: tangency of the pads)
- Microvia placement superimposed to the core via is not recommended
  - If superimposing microvias above the core via cannot be avoided, concentric placement is advised
- Plugging paste and high copper thickness reinforce the core via, which can result in rotational stress on the microvia stack
- Areas of high-resin content surrounding the microvia can exert additional stress on the microvia
- Tightly spaced microvias act as rivets [G. Partida]





LESSONS LEARNT ON MICROVIAS

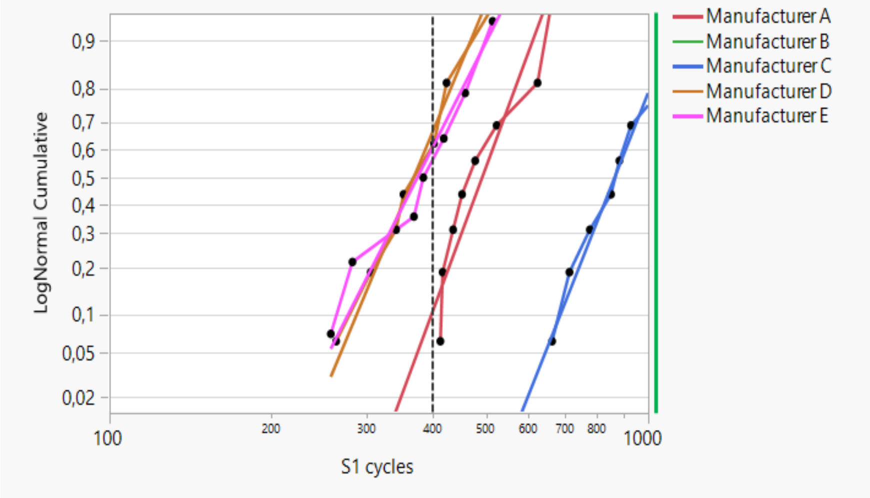
GENERAL RECOMMENDATIONS

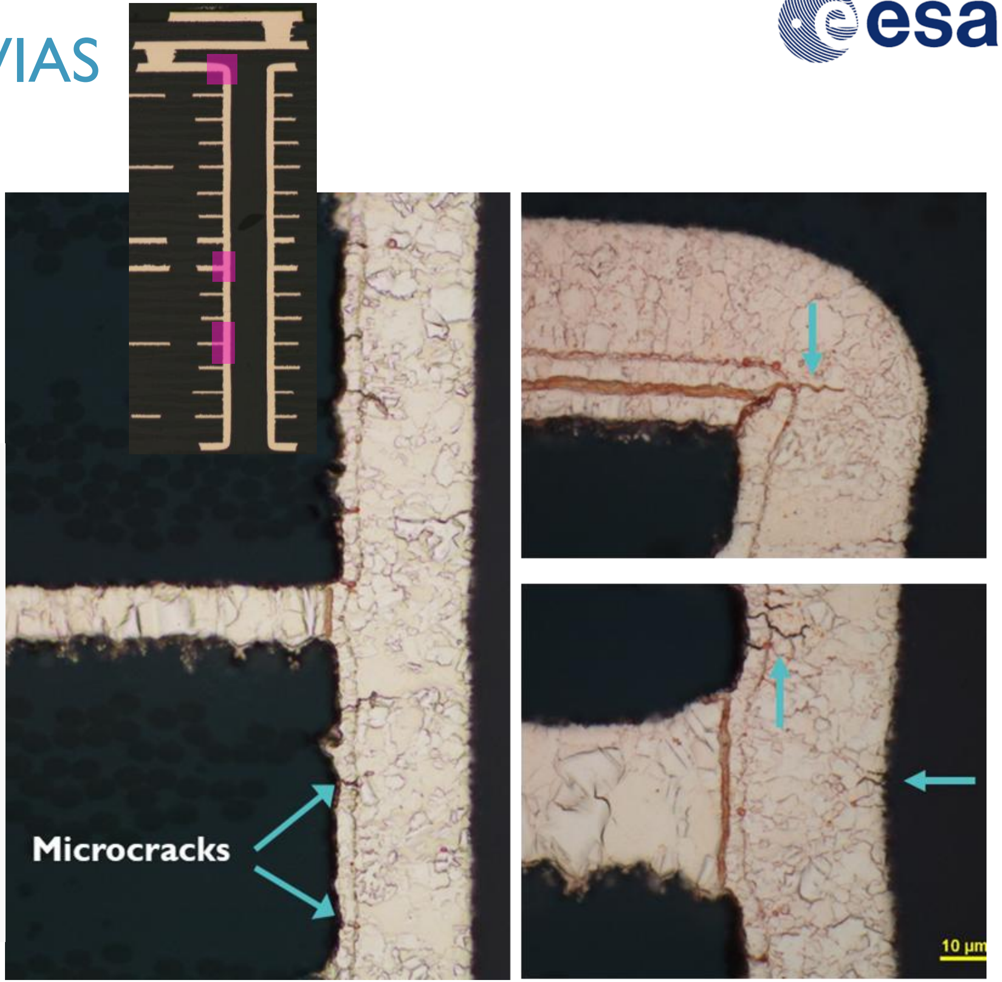
- A through review of manufacturing processes is key to achieving high-quality microvias
- Careful design can dramatically improve the robustness of the microvia
  - Staggered microvias are less likely to fail, but do not ensure safe passage
  - Three levels of stacked microvias will not reduce the reliability of the HDI PCB if designed carefully, manufactured properly and assembly is performed with caution
- All accelerated test methods can differentiate between microvia configurations and be used to assess the capability of a manufacturing process
- A thorough understanding of the impact of design variables, manufacturing processes and test parameters is more important than the choice of microvia test method

LESSONS LEARNT ON COREVIAS

EARLY FAILURES

- Microcracks observed after thermal cycling (Polyimide, △T = 200 °C)
- Interconnect stress testing does not reach requirement of 400 cycles

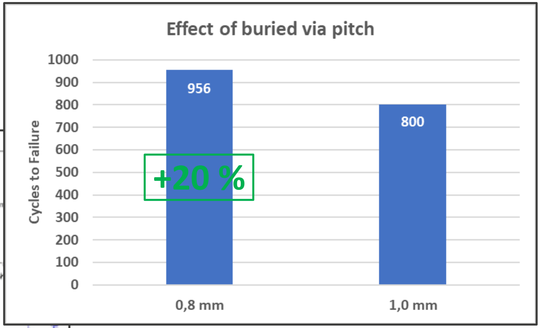


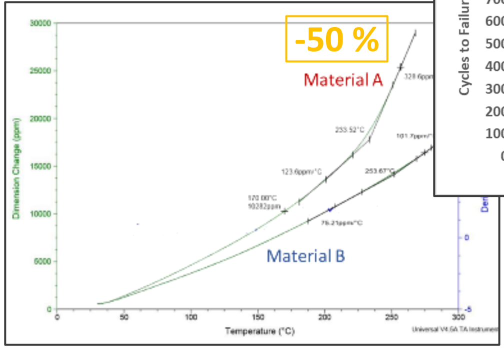


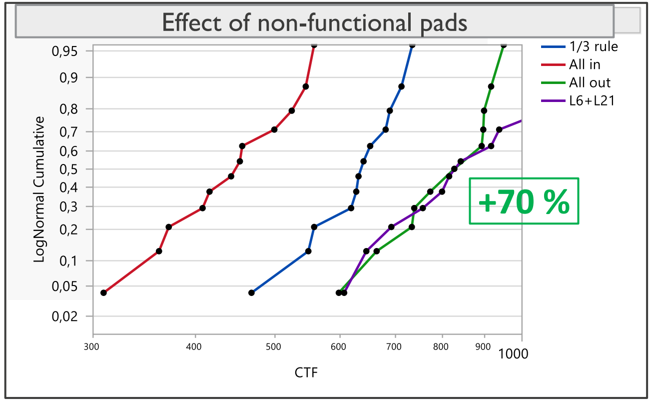
LESSONS LEARNT ON CORE VIAS

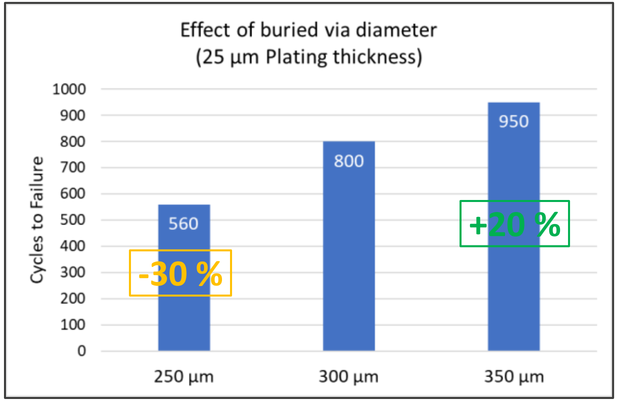
CONTRIBUTING FACTORS

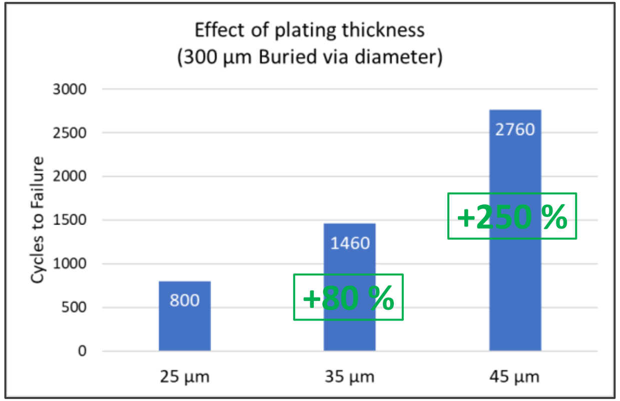
- Failure mechanism for buried vias differs from (unfilled) through holes
- Contribution from design, material choice, manufacturing parameters and end-use environment conditions











LESSONS LEARNT ON CORE VIAS

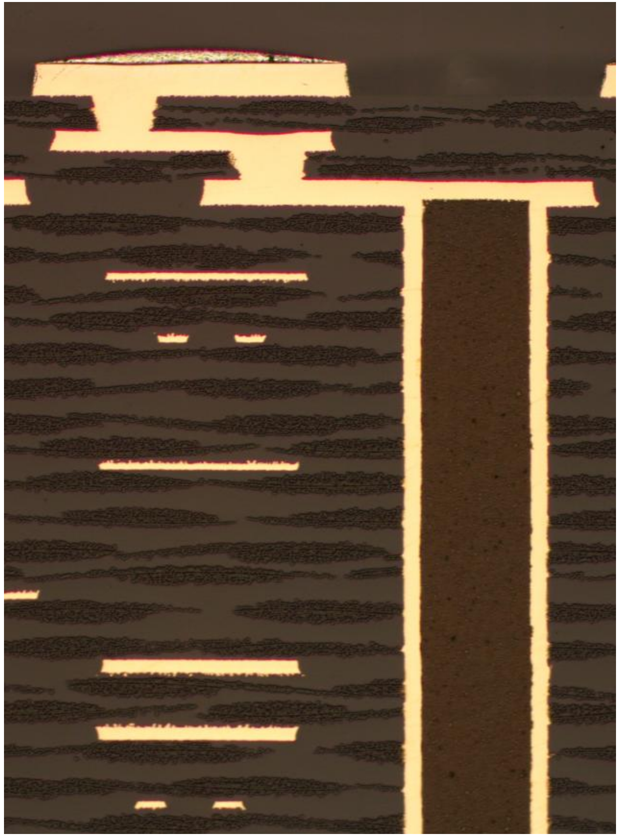
GENERAL RECOMMENDATIONS

- The thermal expansion of the base material remains of key importance
- A core via with a larger diameter is inherently stronger and easier to manufacture
- A higher plated copper thickness inside the core via improves reliability (until it doesn't)
- While a smaller pitch results in higher endurance, do not use as a design feature
- Removing non-functional pads increases the endurance of the core via
- The thermomechanical properties of the material inside the core via need to be match to those of the base material
  - If the resin of the base material can be used to fill the core via, the isotropic expansion of that resin can introduce early failures
  - Using a plugging paste typically creates a stronger barrel, which can have a negative impact on its surroundings

QUALIFIED HDI PCB TECHNOLOGY FOR SPACE APPLICATIONS

ESA's new dimension in printed circuit design

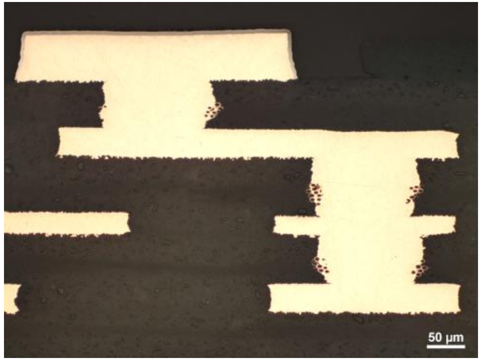
PCB manufacturer ACB in Dendermonde, Belgium, has received ESA qualification for HDI PCBs, as the successful outcome of a recent General Support Technology Programme contract led for ESA by Belgian research institute IMEC, with Thales Alenia Space Belgium as end user.

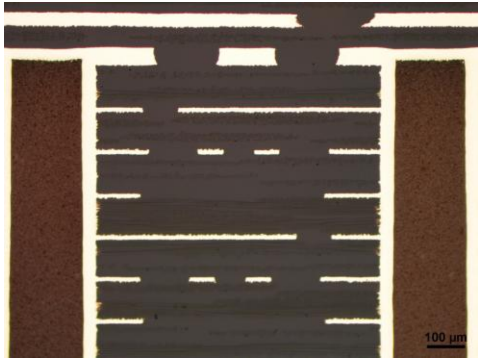


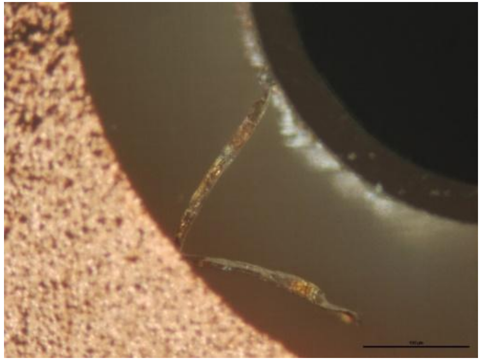
EVALUATION OF COMPLEX HDI TECHNOLOGY

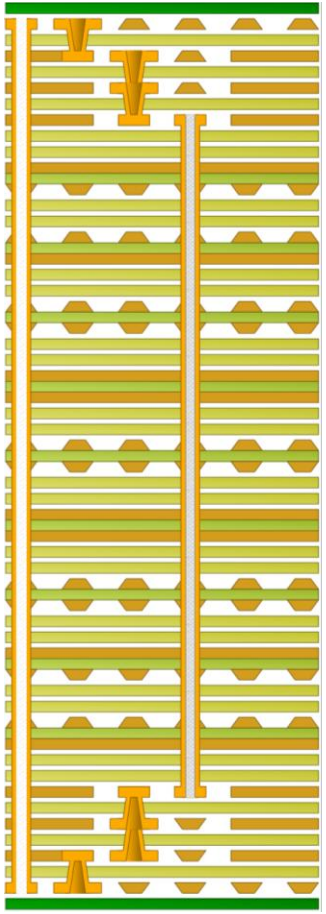
SUMMARY OF RESULTS

- The complex HDI technology introduces several new features, such as stacked microvias, single prepreg, solder mask and new surface finishes
  - Semi-stacked inside microvia configuration passed all the required testing
  - Dielectric thickness control with single prepreg to be further optimized
  - High aspect ratio buried vias with plugging and cap plating remain a challenge
  - Dielectric cracks in RF material observed after testing
  - CAF performance is good, although cleanliness remains a concern









HDI PCB TECHNOLOGY FOR SPACE APPLICATIONS

REVISION OF ECSS STANDARDS ON PRINTED CIRCUIT BOARDS


ECSS-Q-ST-70-12C Rev.1
30 April 2025

EUROPEAN COOPERATION
ECSS
FOR SPACE STANDARDIZATION

Space product assurance

Design rules for printed circuit boards

ECSS Secretariat
ESA-ESTEC
Requirements & Standards Section
Noordwijk, The Netherlands


ECSS-Q-ST-70-60C Rev.1
30 April 2025

EUROPEAN COOPERATION
ECSS
FOR SPACE STANDARDIZATION

Space product assurance

Qualification and procurement of printed circuit boards

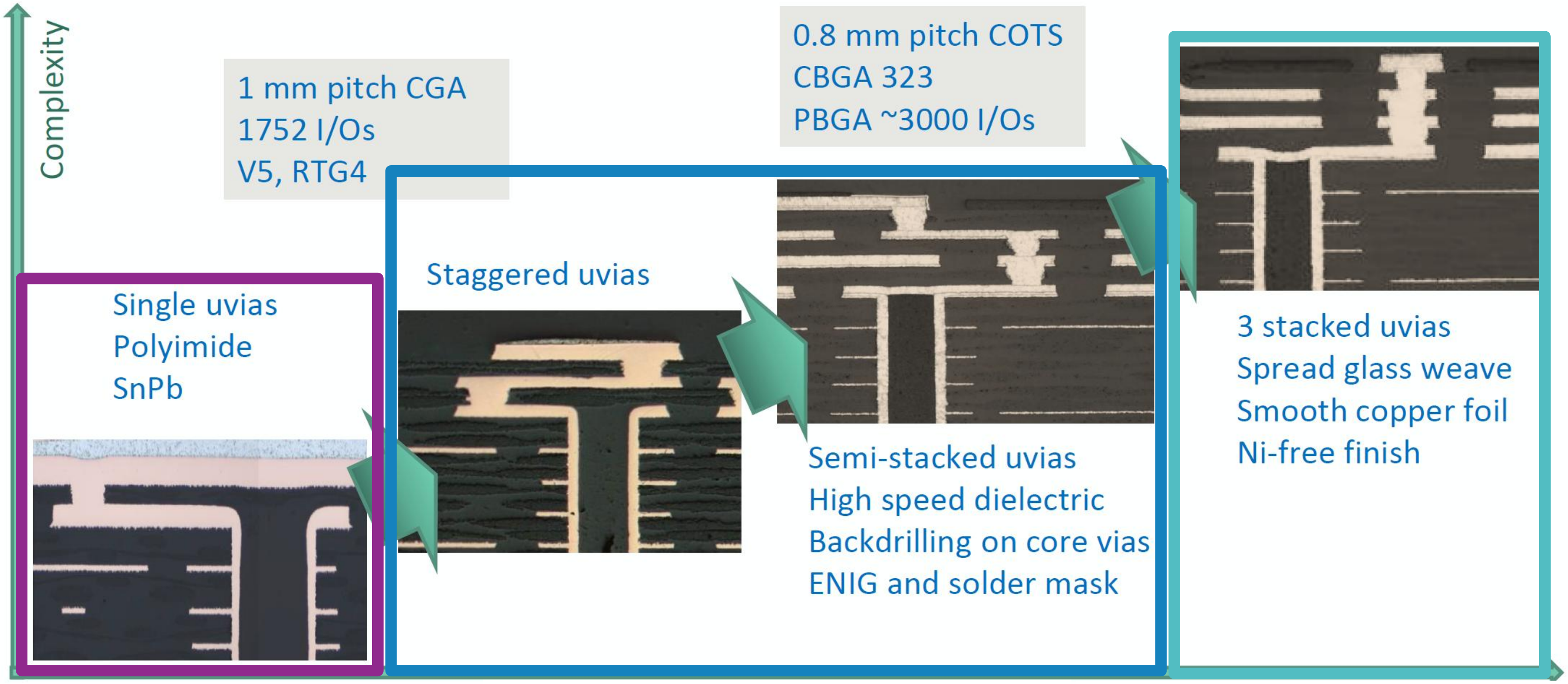
ECSS Secretariat
ESA-ESTEC
Requirements & Standards Section
Noordwijk, The Netherlands

ECSS-Q-ST-70-12C Rev.1

ECSS-Q-ST-70-60C Rev.1

HDI PCB TECHNOLOGY FOR SPACE APPLICATIONS

DEVELOPMENT ROADMAP



ECSS-Q-ST-70-14C 6.25 Gbps

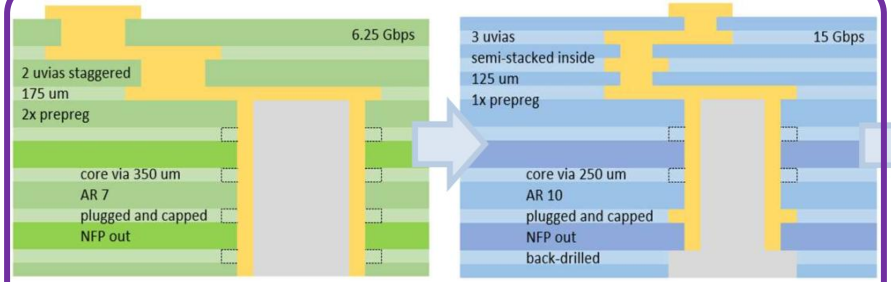
Basic HDI : Qualified
Complex HDI : ready for qualification

HSHDI project objectives:
Qualify, Verify, Evaluate & Investigate

HIGH-SPEED HIGH-DENSITY INTERCONNECT

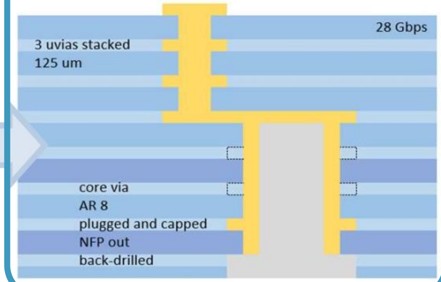
INTRODUCTION

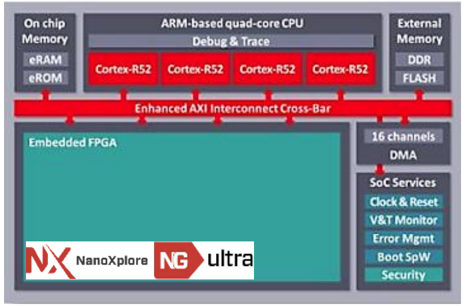
- The need for on-board data processing is increasing strongly
- HDI technology increases the routing density to allow interconnecting high pin-count devices with reduced pitch
- High-Speed HDI technology enables signal and power integrity needed for higher data transfer rates and to accommodate high-performance components



Previous HDI PCB activities

HSHDI project





HIGH-SPEED HIGH-DENSITY INTERCONNECT

PROJECT CONCEPT

Driving components

- High pin count (>2000)
- High speed (>26Gb/s)
- Fine pitch (0.5-1.0 mm)

Technology parameters & design requirements

- Line width and spacing
- Microvia configuration
- Core via aspect ratio
- Base material & build-up
- Back drilling
- Surface finish

Evaluation Test vehicle

HSHDI Technology derisking

Test plan ⇨ Design ⇨ Manufacturing ⇨ Testing

Qualification Test vehicle

HSHDI Technology qualification

Test plan ⇨ Design ⇨ Manufacturing ⇨ Testing

Assembly Test vehicle

HSHDI assembly evaluation

Test plan ⇨ Design ⇨ Manufacturing ⇨ Testing

Design for X

- Modeling-based design
- Parameter prescreening
- Material characterization
- Manufacturing de-risking
- Process and cleanliness review

Conclusions

- Result analysis
- Lessons learnt

HSHDI TECHNOLOGY DEFINITION
DRIVING COMPONENTS

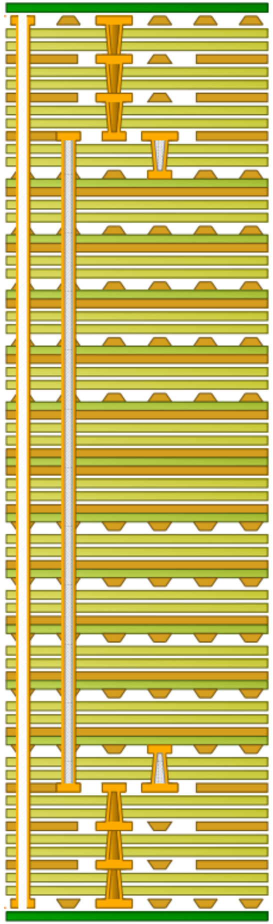
- High pin count (<2000), high speed (>26Gbps), 0.8/0.92/1.0 mm-pitch BGAs, ceramic and plastic
  - FPGAs such as NanoXplore NG Ultra & AMD Xilinx Versal with high-speed serial links (HSSL)
  - New generation of ADC and DAC – lower pin count (<200) with smaller pitch (0.8 mm)
- Small pitch BGAs (0.5 mm) with lower pin count (<200)
  - Memory devices and future RF packages
- Board-to-board connectors
  - cCPI serial connectors (12.5 – 25 Gbps)
  - Press fit and S-FECT connection technology
- 0201 capacitors for decoupling

	Basic HDI technology		High-speed HDI	
	Xilinx Virtex 5QV	Microchip RTG4	NanoXplore Ultra	AMD Xilinx Versal
Package	CCGA, 1752 I/Os, 1.0 mm pitch	CCGA, 1657 I/Os, 1.0 mm pitch	PBGA, 1760 I/Os, 1.0 mm pitch	PBGA, 2197 I/Os, 0.92 mm pitch
HSSL	24x 6.25 Gbps	24x 3.125 Gbps	32x 12.5 Gbps	44x 25 Gbps
Power	10 W	5 W	Up to 50 W	50-100 W

HSHDI TECHNOLOGY DEFINITION

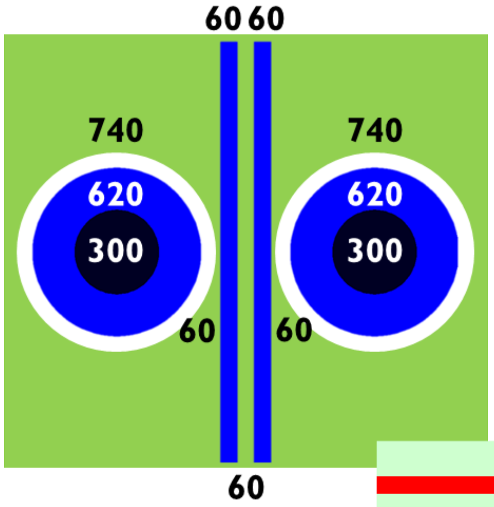
TECHNOLOGY PARAMETERS FOR HIGH-SPEED HDI TECHNOLOGY

HDI technology parameter	high-speed HDI	Motivation
Conductor width and spacing, as-designed	Non-plated : 50/50 µm on 17 µm Cu foil; Plated : 100/100 µm on 12 µm + (1x25)	Differential pair routing; Foil thickness for min R and risk of ICD; High-speed routing on outer layer
Configuration of microvias	3.5 levels of microvias (3x Cu filled + 0.5 plugged); Three levels stacked and 0.5 level staggered; 150 µm drill diameter	Microvia layers as reference planes & direct access to first high-speed layer; Stacked for optimize routing; Reduced aspect ratio and higher contact area
Number of layers	≤ 30	Number of high-speed routing layers
Construction of HDI layers	Staggered to core; two sheets of prepreg; 35 ± 5 µm Cu (40 ± 10 µm on core)	Staggered for higher reliability; Dielectric thickness for microvia layers; Min Cu for power delivery, max for dielectric thickness
Aspect ratio of core vias	≤ 9	Compromise between design needs and reliability
PCB thickness	Approx. 3 mm, 75 µm dielectric thickness in core	Reduced dielectric thickness to minimize total thickness
Filling medium for core vias	Via plugging (with cap plating)	Increased reliability
Construction of core	Single sequence; 250 µm drill (0.8 mm pitch) & 300 µm (0.92-1.0 mm pitch)	Single sequence to reduced complexity and better registration; Pad defined by differential pair routing
Back drilling	Back drilling on core and PTH	Improved high-speed performance
Presence of non-functional pads	Full pad stack removed on core vias and PTH, except for component holes	Improved high-speed performance, with reinforcement for manual soldering
Dielectric material	High-speed base material from 2 suppliers	High-speed performance, thermomechanical properties, manufacturing heritage, supply chain
Surface finish and solder mask	ENIG with solder mask	Manufacturing heritage and logistical ease

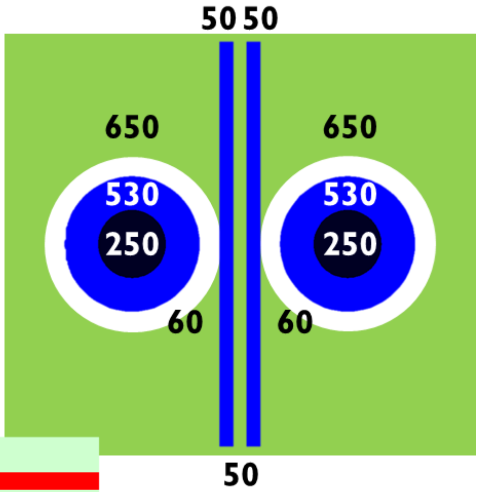


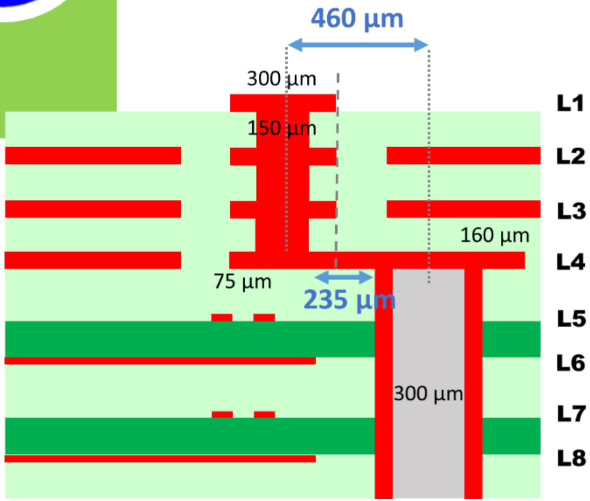
TECHNOLOGY PARAMETERS FOR HSHDI

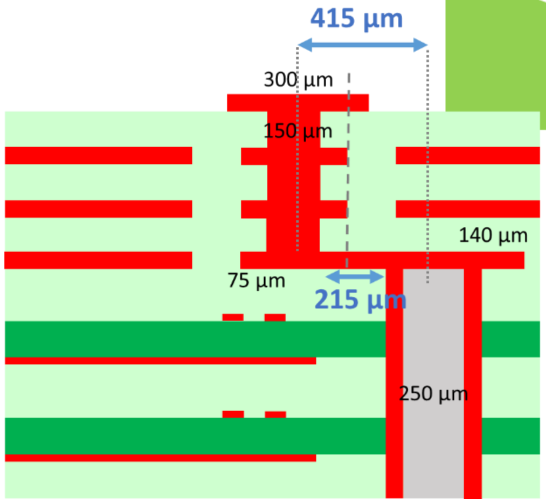
REFERENCE DESIGN CONFIGURATIONS



The technology parameters are translated into the HSHDI reference design configurations for 0.8 mm and 0.92 mm pitch, defining core via drill diameters, microvia drill diameter, pad sizes and positioning of the microvia stack with respect to the core via





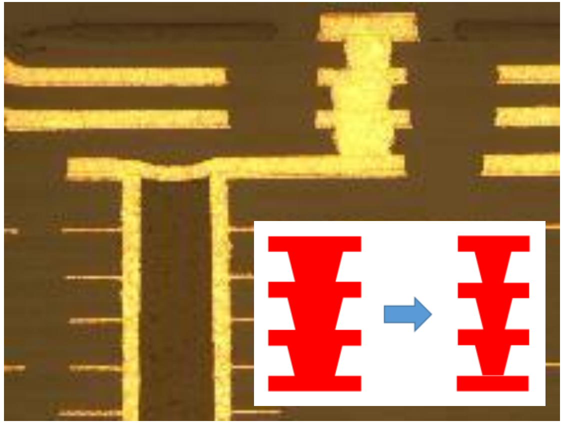


0.92 mm pitch

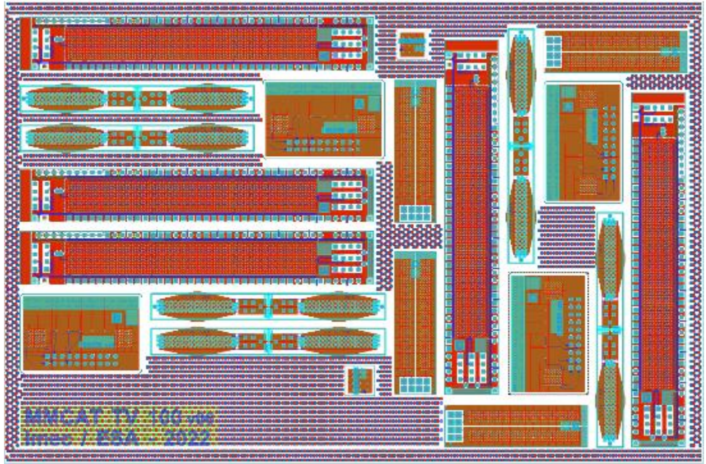
0.8 mm pitch

HDI PCB TECHNOLOGY FOR SPACE APPLICATIONS

EU IPC UVIA WORKING GROUP



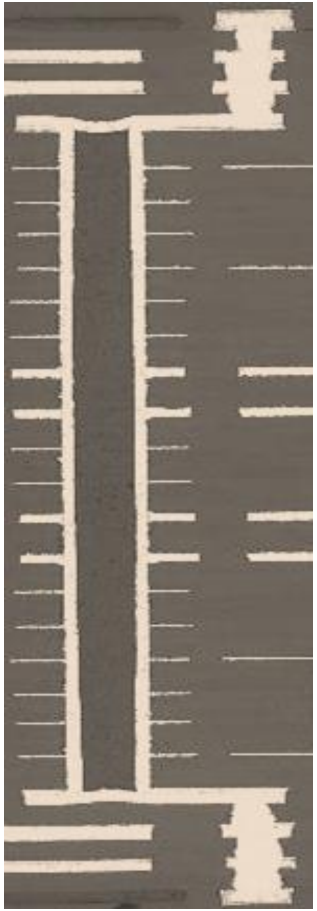
- PCB experts from EU high-rel electronics manufacturing industry jointly address the microvia reliability concern
- Execute a round-robin campaign using a standard test panel based on consolidated design drivers
  - Three stacked microvias, off-set to core via (~90% of high-rel)
- Validate test methodology by evaluating all relevant accelerated coupon test methodologies
  - IST, CITC, HATS2 and OM testing
- Benchmark manufacturing capability by step-wise reduction of microvia drill diameter
  - Ø 175, 150, 125, 100 um in 100 um dielectric
- Contact Stan.Heltzel@esa.int in case of interest



HDI PCB TECHNOLOGY FOR SPACE APPLICATIONS

EU IPC UVIA WORKING GROUP

- PCB experts from EU high-rel electronics manufacturing industry jointly address the microvia reliability concern
- Focus on high-reliability applications (aerospace, defence, oil drilling…)
- Consolidated design drivers
  - Stacked microvias provide the highest routing density
  - Three levels of stacked microvias covers the majority of high-rel HDI designs
  - Core construction shall be representative of high-rel HDI designs
- Validate test methodology
  - Execute a round-robin campaign using a standard test vehicle
  - Evaluate all relevant accelerated coupon test methodologies
  - Cross reference results with qualitative metallurgical assessment
- New capability test methodology to quantify microvia robustness and assess margin of microvia processes from PCB manufacturers

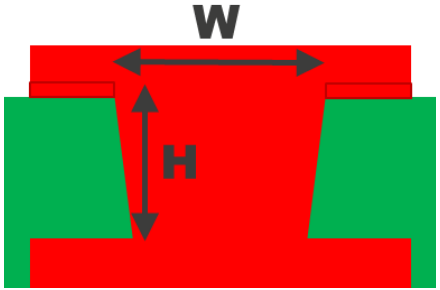


IPC-V-TLS-MVIA-EU WORKING GROUP

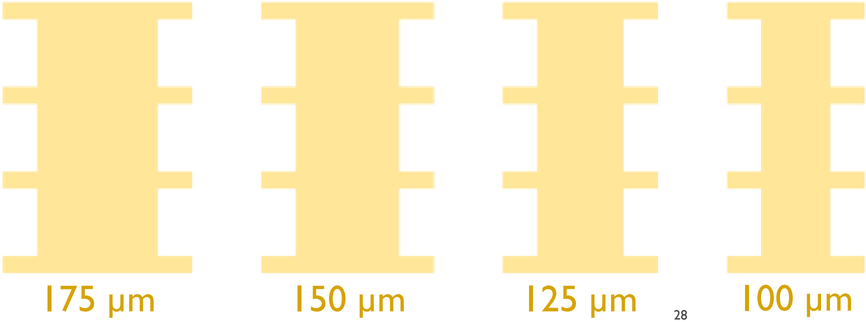
MICROVIA MANUFACTURING CAPABILITY ASSESSMENT

METHODOLOGY

- Benchmark manufacturing capability by **step-wise reduction of microvia drill diameter** for a fixed dielectric thickness
  - Reduced microvia diameter leads to increased routing density
  - High aspect ratio impacts flow of process chemistry
  - Smaller cross-sectional area results in reduced strength
- Four microvia diameters to verify expected trend
  - Smallest diameter is deliberately out of the manufacturer's comfort zone to assess the margins of the process window



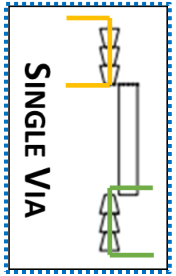
100 µm dielectric + Cu foil	
Diameter	**Aspect ratio**
175 µm	0.7
150 µm	0.8
125 µm	0.9
100 µm	1.2

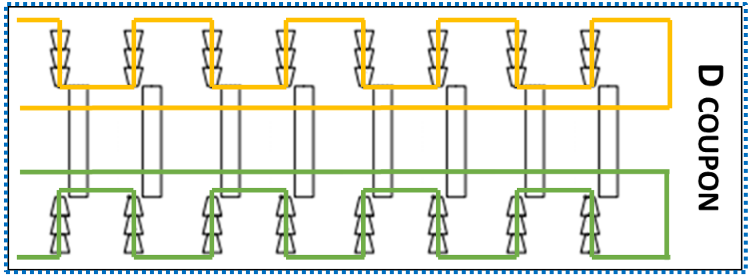


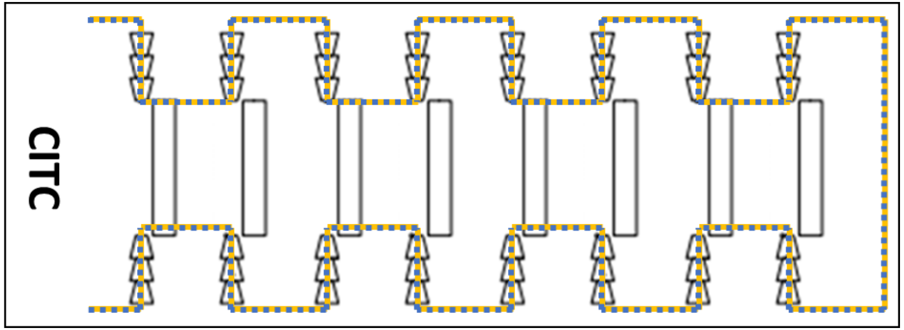
MICROVIA MANUFACTURING CAPABILITY ASSESSMENT

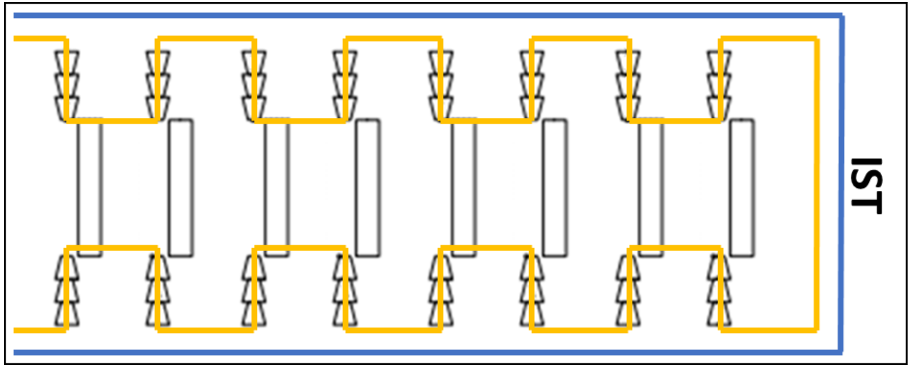
ACCELERATED COUPON TEST METHODOLOGIES

- Convection reflow assembly simulation followed by air-to-air thermal shock
  - Performed on daisy chained D-coupons and on HATS^2 single via coupons
  - IPC-TM-650 2.6.27B and 2.6.7.2C
- Interconnection stress testing (IST)
  - IPC-TM-650 2.6.26, method A & ECSS-Q-ST-70-60C
- Current-induced thermal cycling (CITC)
  - IPC-TM-650 2.6.26, method B







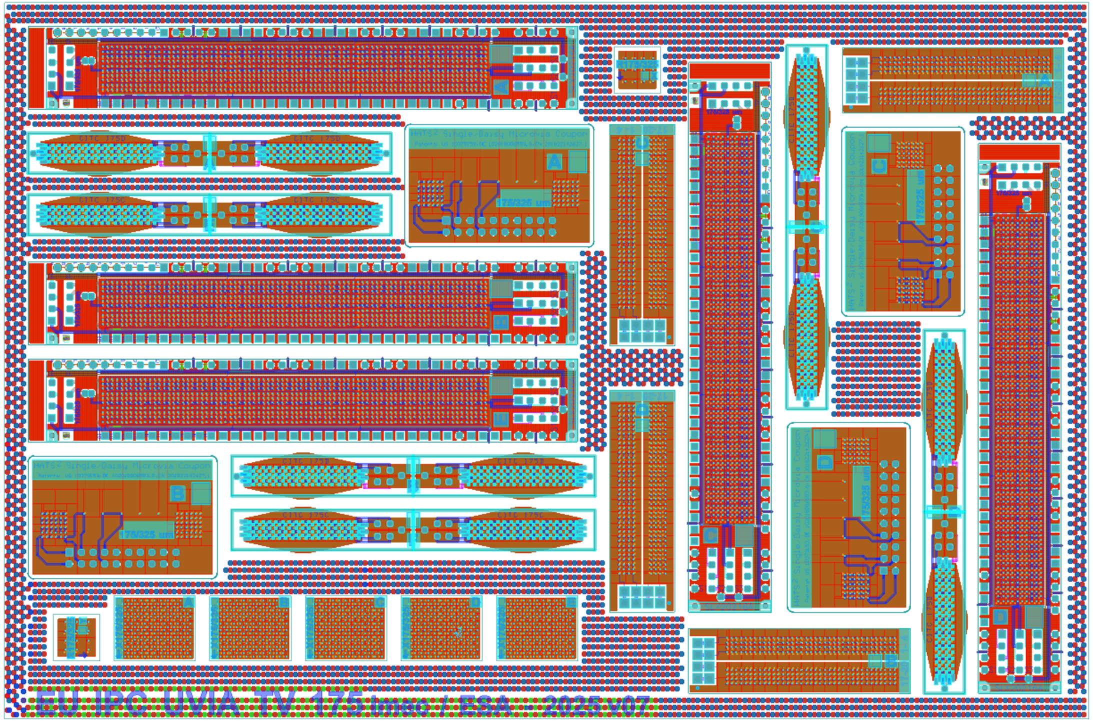


MICROVIA MANUFACTURING CAPABILITY ASSESSMENT

TEST VEHICLE DESIGN

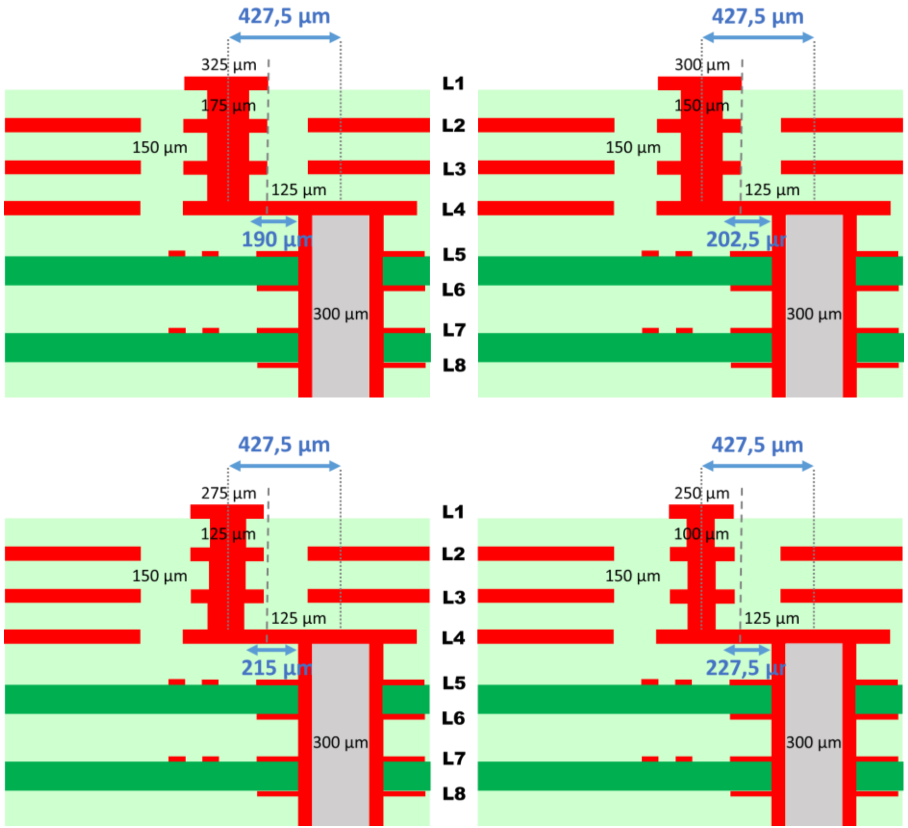
- All coupons are grouped on a single test vehicle per diameter to better resemble a real HDI PCB design and assure consistency between manufacturers
- **One test vehicle per microvia diameter**, including:
  - 5 IST coupons (1 spare)
  - 6 CITC coupons
  - 4 HATS2 coupons
  - 4 D coupons
  - 2 registration coupons
  - 5 microsection coupons
- Material analysis coupon separate
- Test vehicle to be treated as PCB by the manufacturer
- Unique identifier per coupon

235 mm x 150 mm



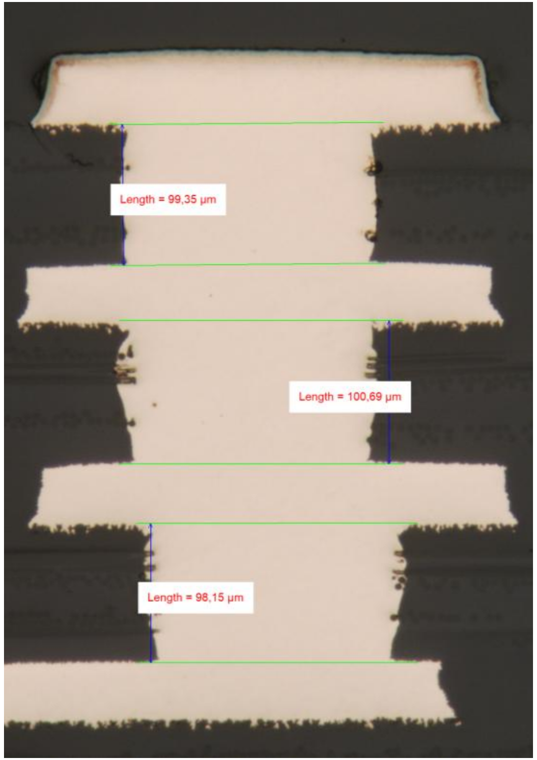
TEST VEHICLE DESIGN
MICROVIA DESIGN PARAMETERS

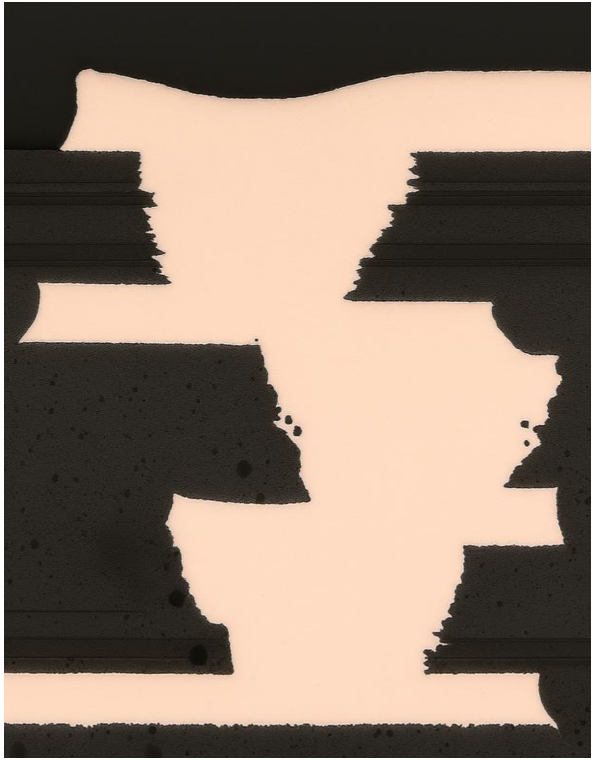
- Core vias included to represent reality
- Distance between microvia stack and core via is contributing factor to microvia stress
  - Design rule: tangency of the pads
  - For consistency of testing across microvia diameters, the distance is kept constant
- Pad diameter is adjusted to drill diameter
  - ECSS-Q-ST-70-12C rev1 design rules
- A larger pitch results in higher stress
  - Common pitch for high-rel: 0.8 – 1.0 mm
  - 1.0 mm pitch is considered worst-case
- Core vias are plugged and cap plated



1ST ROUND OF TESTING ON POLYIMIDE

NOT ALL MICROVIAS ARE CREATED EQUAL



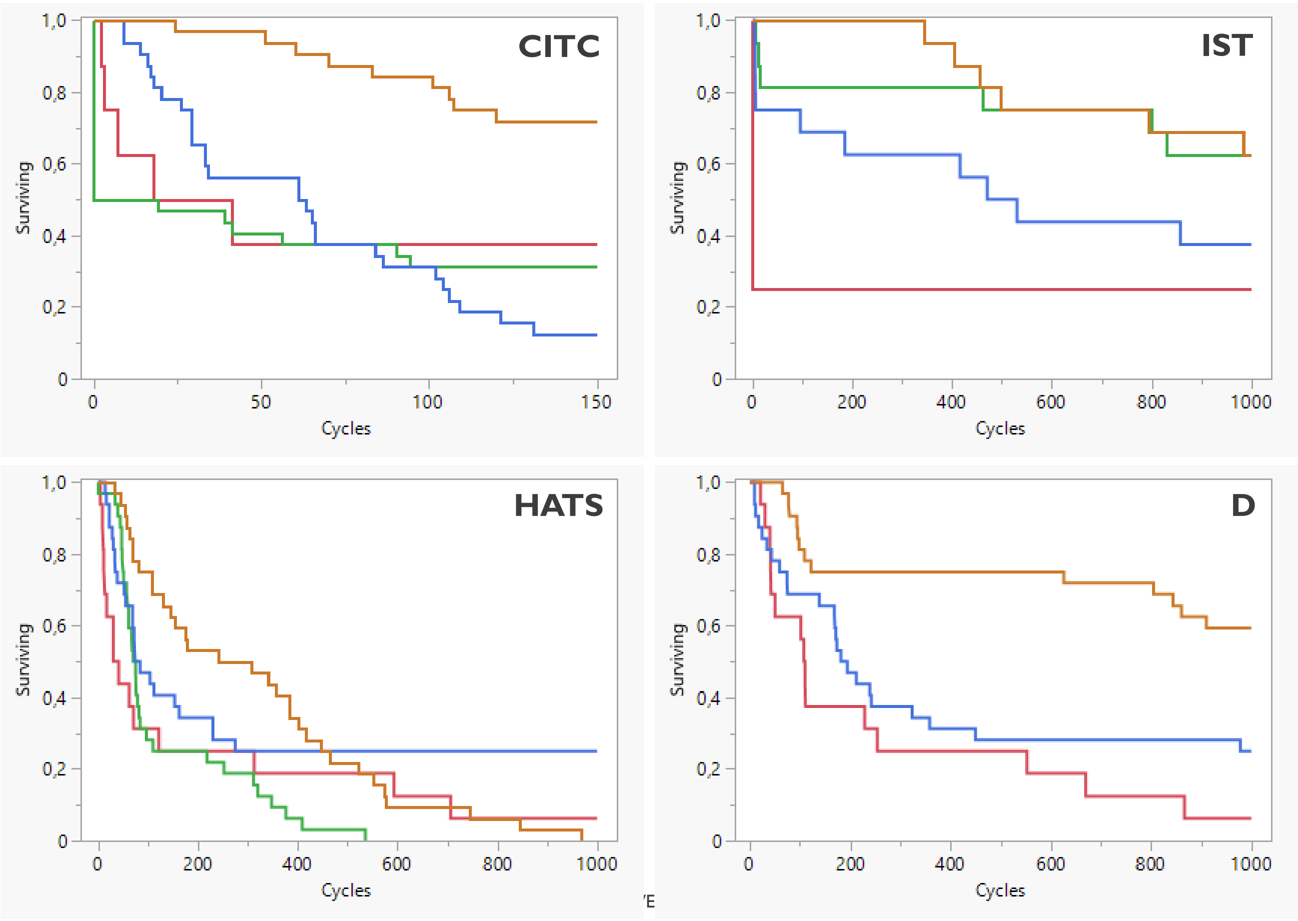


IST ROUND OF TESTING ON POLYIMIDE

TEST RESULTS (SO FAR)

Manufacturer B Manufacturer G
Manufacturer F Manufacturer H

- Smaller microvia diameters fail before larger diameters
  - Smallest diameter shows acceptable performance
  - Large spread in results per diameter
- Manufacturing capability per manufacturer apparent
  - Scoring system needed
  - Number of microvias per daisy chain impacts results
- No major discrepancies between test methods



MICROVIA MANUFACTURING CAPABILITY TEST

CONCLUSION

- Microvia technology is notorious for a latent and intermittent open circuit failure that is difficult to screen
- A new capability test methodology is developed to quantify the robustness and assess margin of the microvia processes from PCB manufacturers
- Test samples were (and will be) received from state-of-the-art PCB manufacturers from Europe, Asia and the United States
- Test samples were (and will be) submitted to four accelerated coupon tests methods, as well as a qualitative metallurgical assessment
- Based on the initial results, the step-wise reduction of microvia drill diameter has proven to be good measure for capability assessment

⇨ If interested in joining EU IPC UVIA Working group, please contact Stan.Heltzel@esa.int or Maarten.Cauwe@imec.be

FURTHER READING

I. M. Cauwe, S. Heltzel, J. Furlong, C. Nawghane, M. Van De Slyeke, and A. Coulon (2021), "Round robin testing of HDI technology from space-qualified PCB manufacturers," *Proceedings of the 21st IPC APEX EXPO*, San Diego, CA.

II. M. Cauwe, C. Nawghane, M. Van De Slyeke, S. Heltzel, J. Furlong, B. Neves, and K. Knadle (2022), "Design and testing of three levels of microvias for high-reliability PCBs," *Proceedings of the 22nd IPC APEX EXPO*, San Diego, CA.

III. M. Cauwe, A. Coulon, C. Nawghane, B. Vandevelde, M. Van De Slyeke, and S. Heltzel (2022), "Microvia technology assessment for space applications," *SMTA Europe Electronics in Harsh Environments Conference*, The Netherlands.

IV. M. Cauwe, S. Heltzel, J. Furlong, C. Nawghane, M. Van De Slyeke, and A. Coulon (2021), "Round robin testing of HDI technology from space-qualified PCB manufacturers," *Proceedings of the 21st IPC APEX EXPO*, San Diego, CA.

V. M. Cauwe, C. Nawghane, A. Coulon, M. Van De Slyeke, and S. Heltzel (2023), "Contributing factors to the reliability of buried vias in high-density interconnect PCBs," *Proceedings of the 23rd IPC APEX EXPO*, San Diego, CA.

VI. M. Cauwe, C. Nawghane, M. Van De Slyeke, and S. Heltzel (2025), "Design for manufacturing and reliability of a high-speed HDI technology for space applications," presented at the Pan-European Design conference (PEDC), Vienna, Austria.

VII. J. Verhegge, M. Van De Slyeke, M. Cauwe, C. Nawghane, and S. Heltzel (2025), "High-speed HDI technology for space applications: a road to qualification," presented at the Electronics Manufacturing & Packaging Symposium (EMPS), ESA-ESTEC, The Netherlands.

VIII. M. Cauwe and S. Heltzel (2025), "Microvia manufacturing capability assessment: a perspective on three levels of stacked microvias," presented at the Electronics Manufacturing & Packaging Symposium (EMPS), ESA-ESTEC, The Netherlands.

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