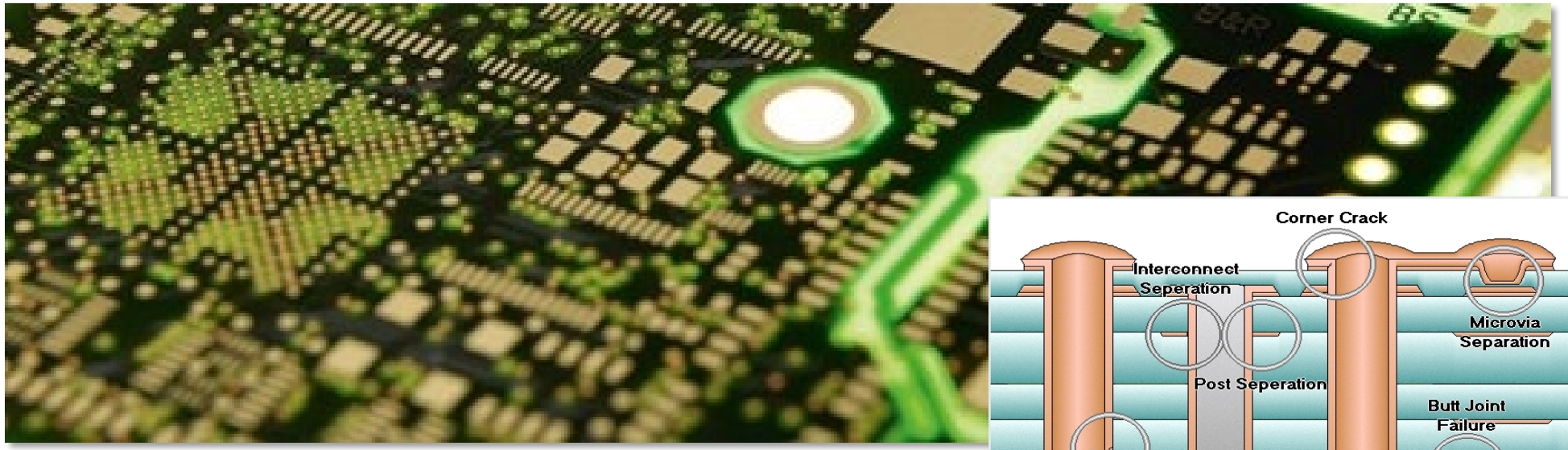
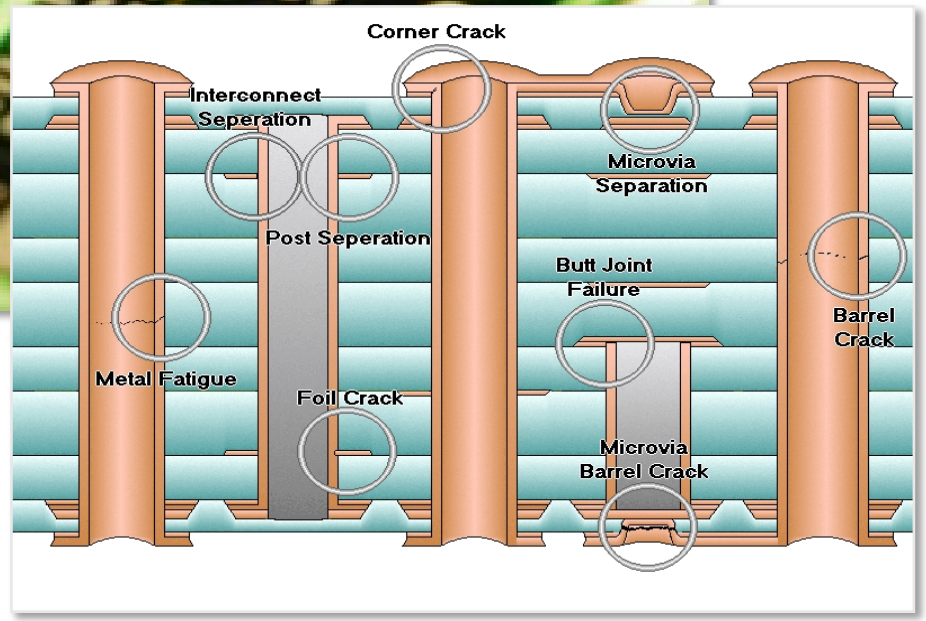
Experiences from IST Interconnect Stress Test – how do PCBs fail?





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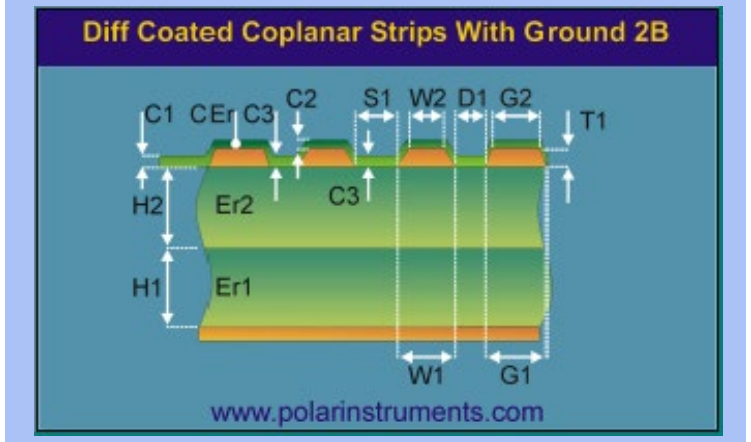
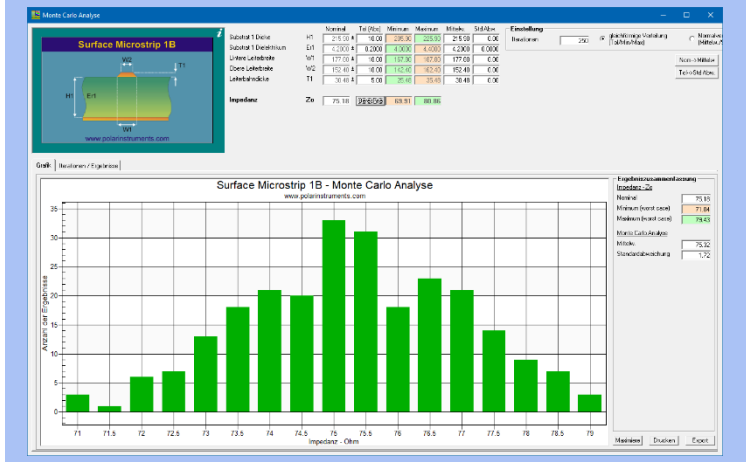
Fax +43 7666 20041-20

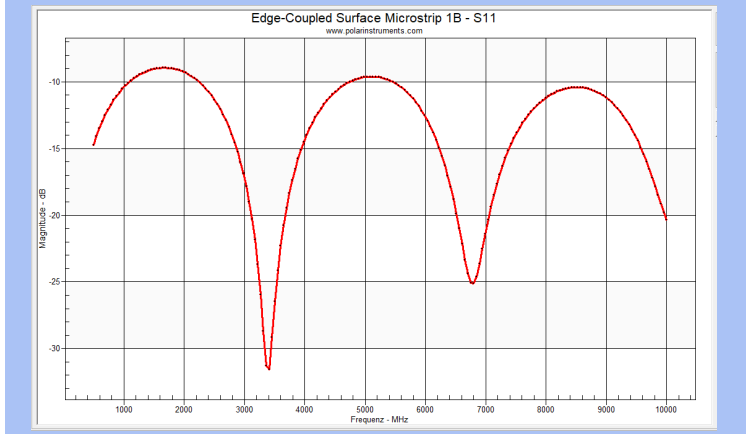
Polar Instruments GmbH - Software

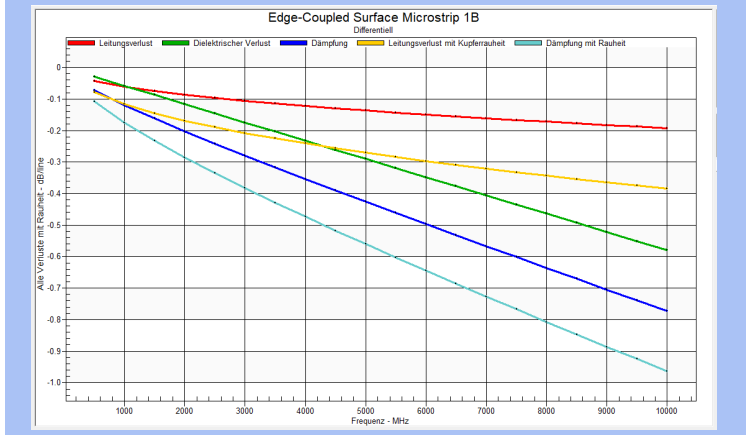
Impedance Calculation



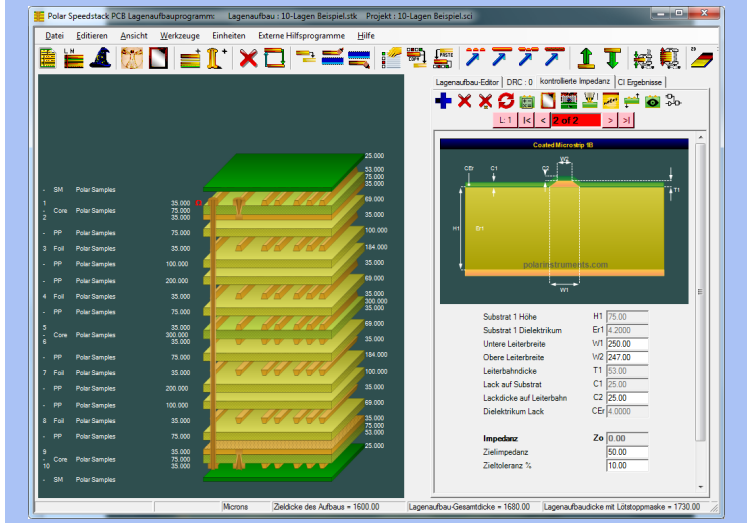


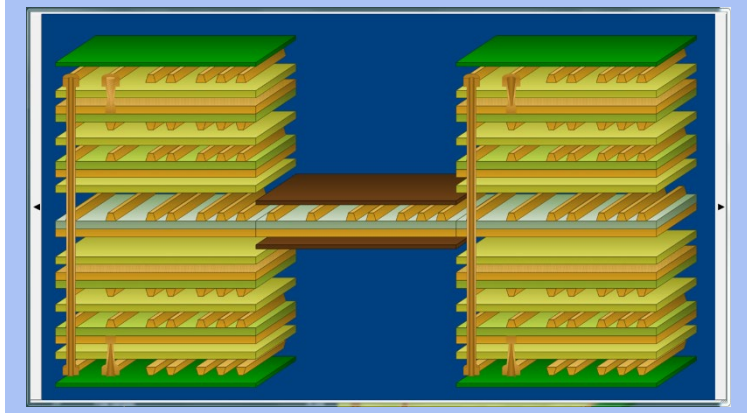
Transmission Line Simulation





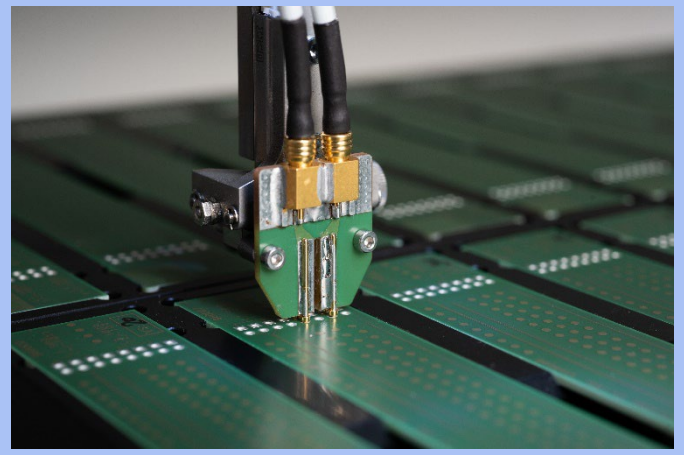
Stackup Documentation

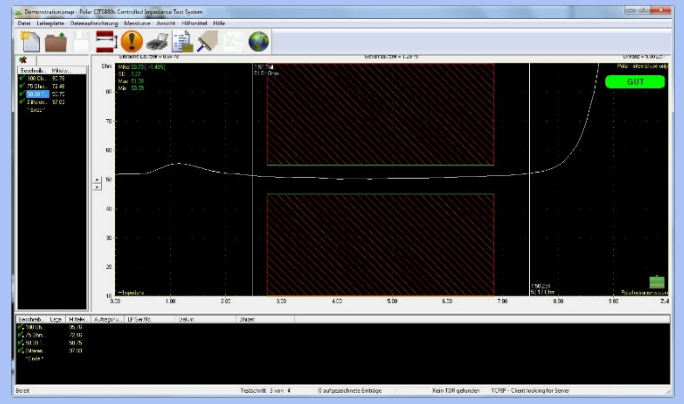




Polar Instruments GmbH - Hardware

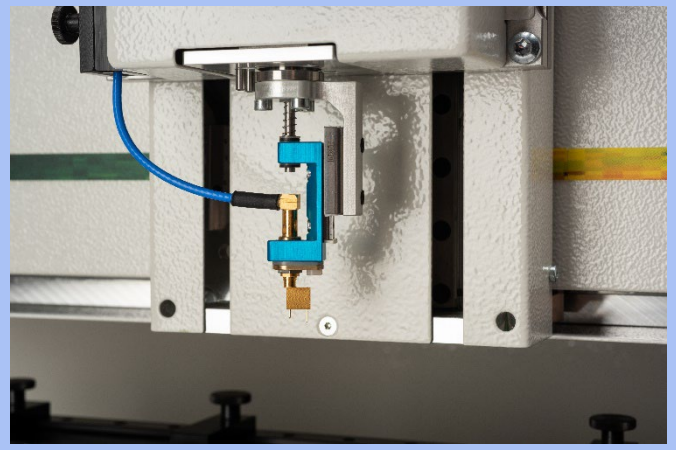
Impedance Measurement

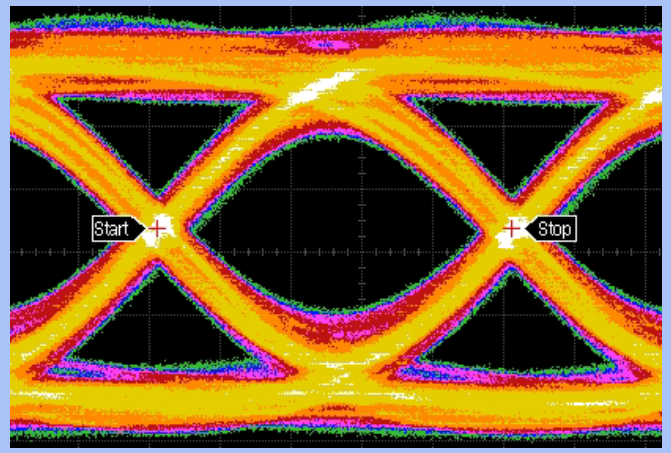




Loss Measurement

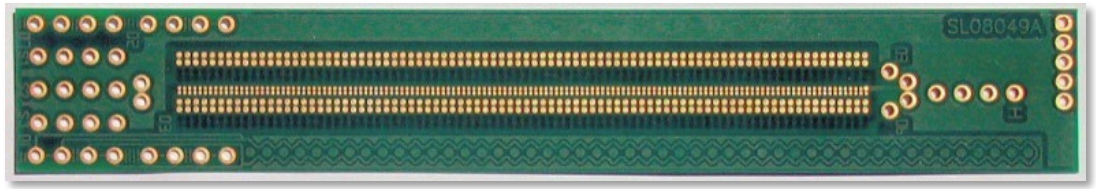
Design Verification

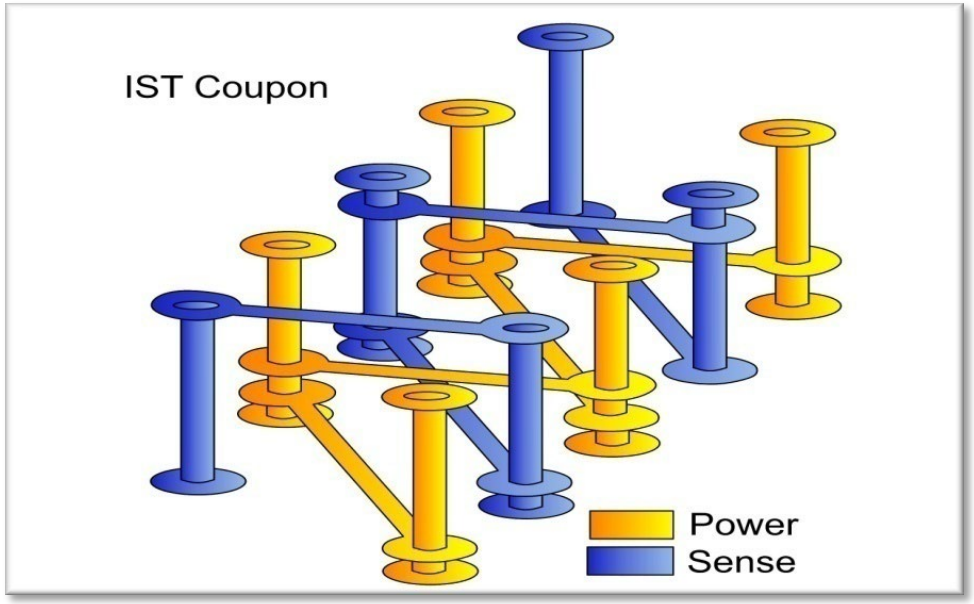




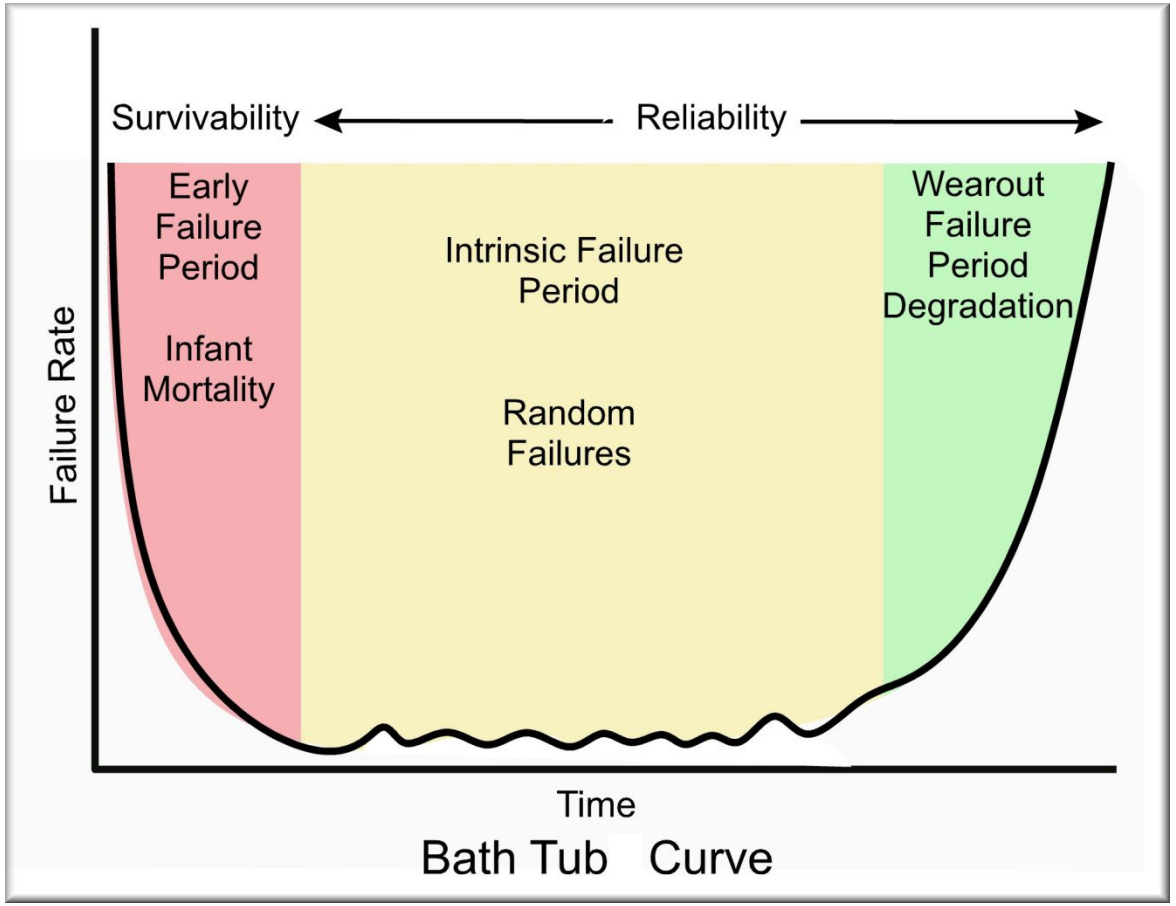
Automated controlled impedance test systems RITS550/RITS880

PCB Reliability Test using IST Interconnect Stress Test:





Definition of Reliability



Reliability is the **probability** that an item will perform its intended function for a specified **time interval** under **stated conditions**.

PCB Reliability Challenges:

Lead Free Solder Process:	Solder temperatures > 260°C
	Hot Air Levelling
	6x Rework
High Reliability Applications:	Medical
	Avionics/Aerospace
	Defense
	Automotive/Transportation

“Survivability” versus “Reliability”:

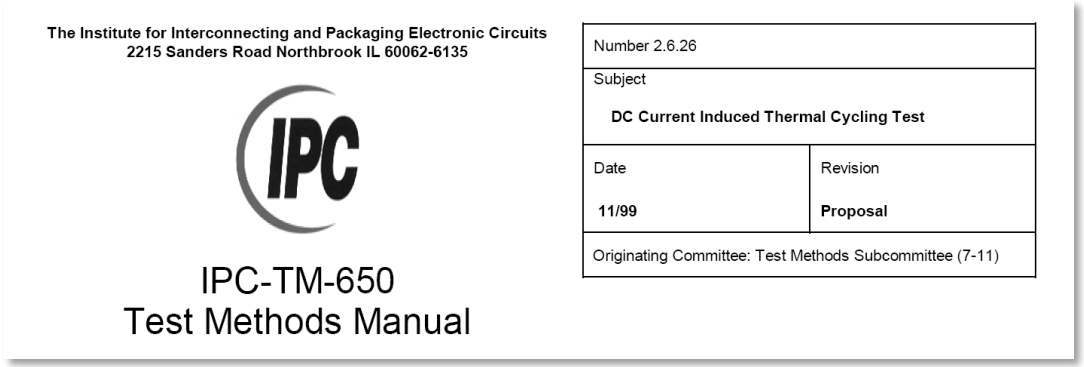
Survivability:
Methodology to establish a products ability to survive the thermal excursions associated with **assembly** and potential **rework** cycles

Reliability:
Methodology to establish a products ability to survive the thermal excursions associated with the **end use environment**

Thermal Shock Test Methods:

Air to Air thermal shock (ATC) – Air to Air Thermal Shock – Method 2.6.7.2A (15 min @ 125°C/15 min @ -35°C.

IST Interconnect Stress Test - Current Induced Thermal Shock – Method 2.6.26 (3 min to 150°C/2 min to 20°C



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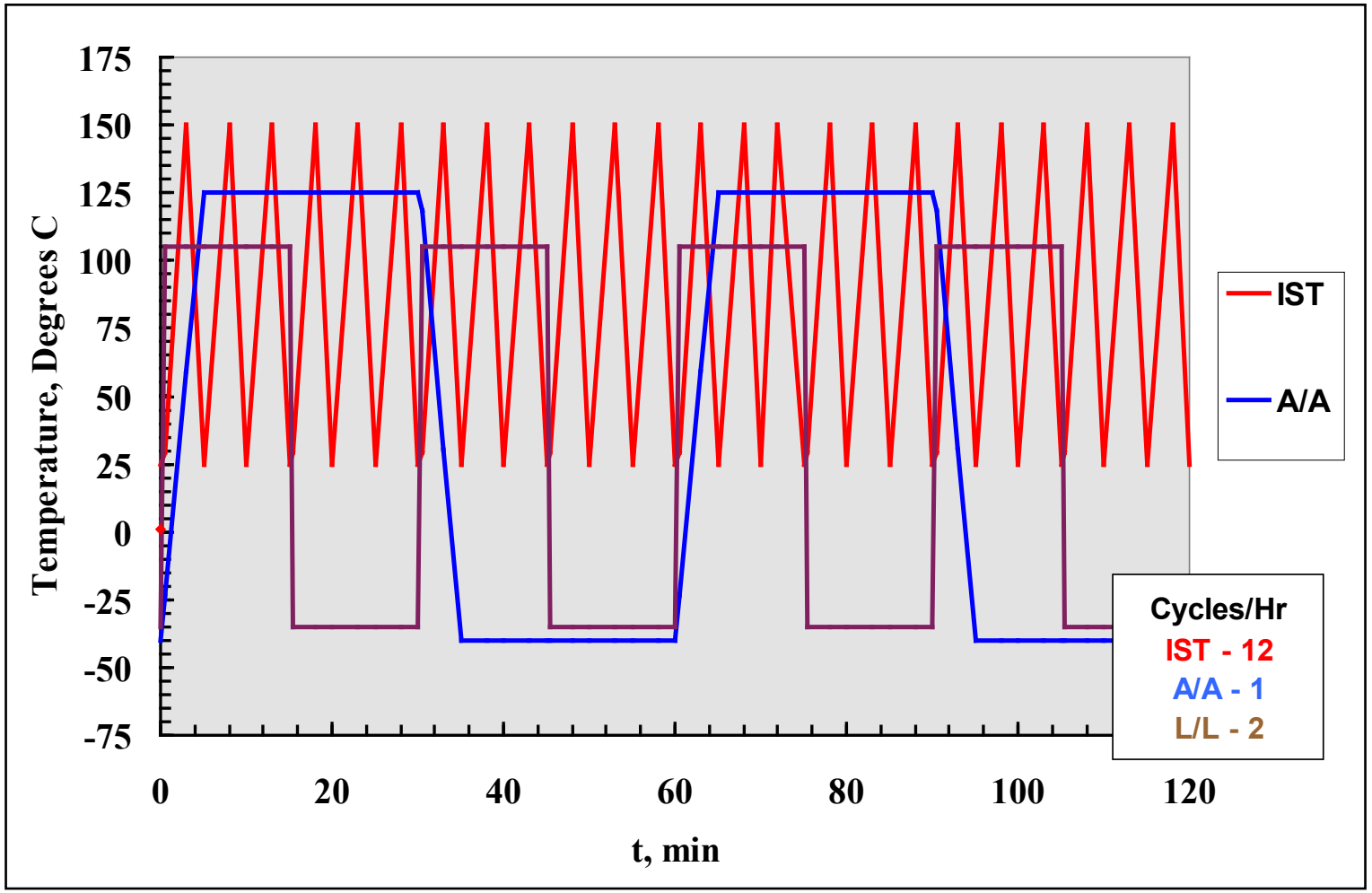
IPC-TM-650
Test Methods Manual

Number 2.6.26	
Subject **DC Current Induced Thermal Cycling Test**	
Date **11/99**	Revision **Proposal**
Originating Committee: Test Methods Subcommittee (7-11)	

Comparison IST vs. Oven Test

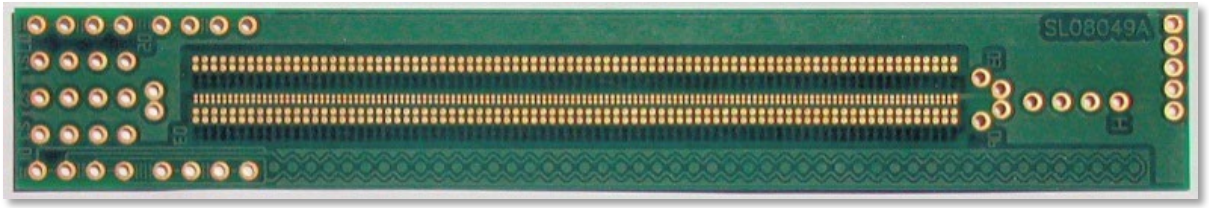


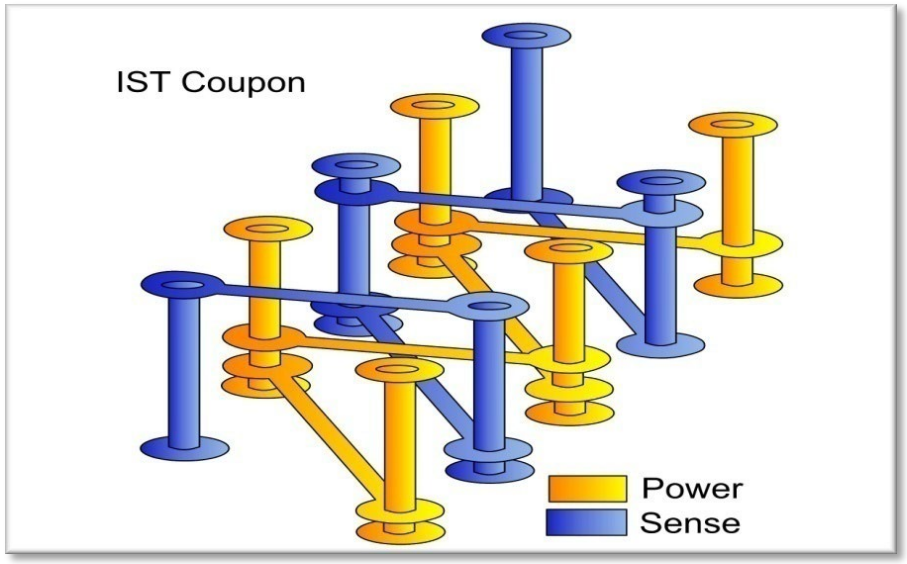
Oven Test: lower maximum temperatures, tests also to negative temperatures, longer dwell times, longer cycle times (1 hour), 1000 cycles ~ 42 days

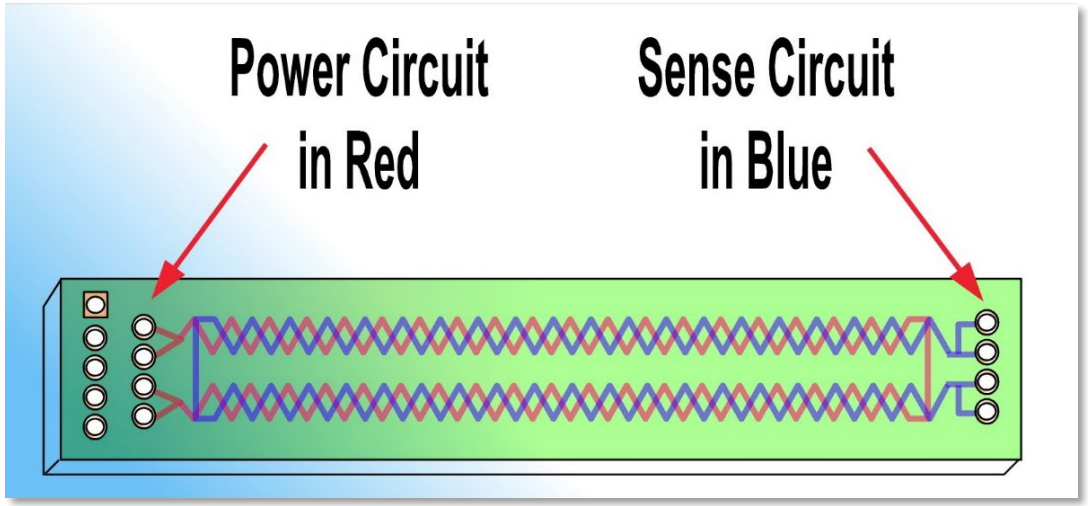
IST: tests from ambient temperature, higher maximum temperatures, no dwell times, very short cycle times (5 minutes)

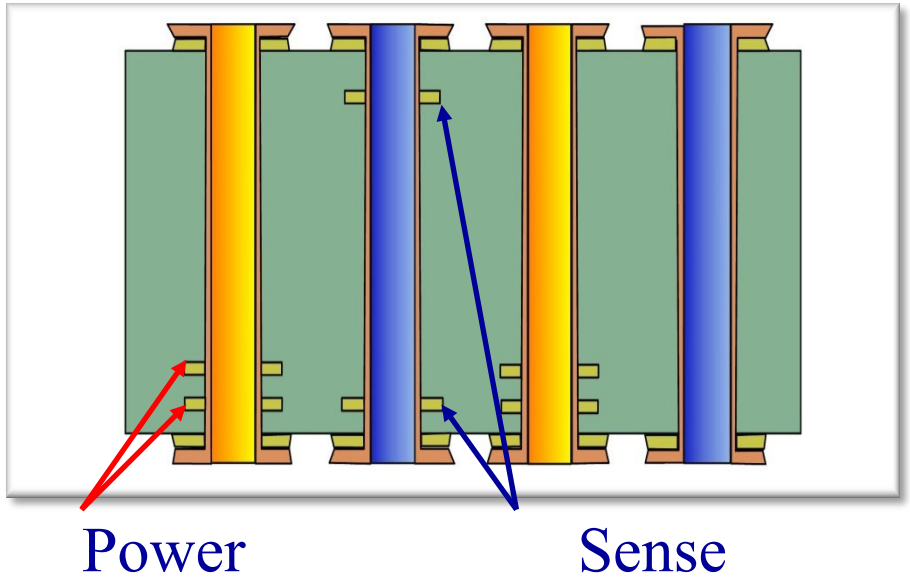
1000 cycles ~ 4 days

IST Test Coupon:

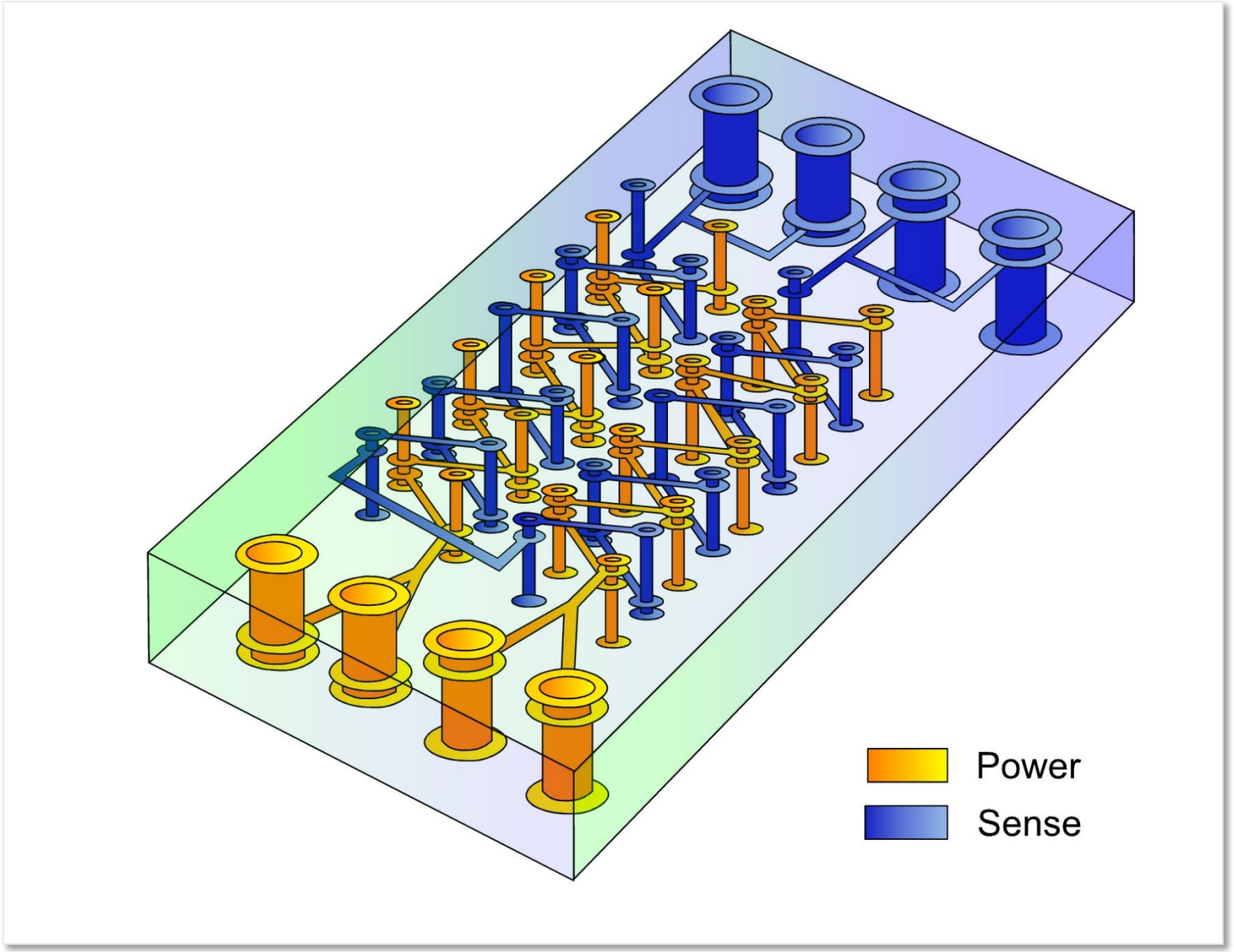








IST Coupon Design Logic – Heating Circuit:



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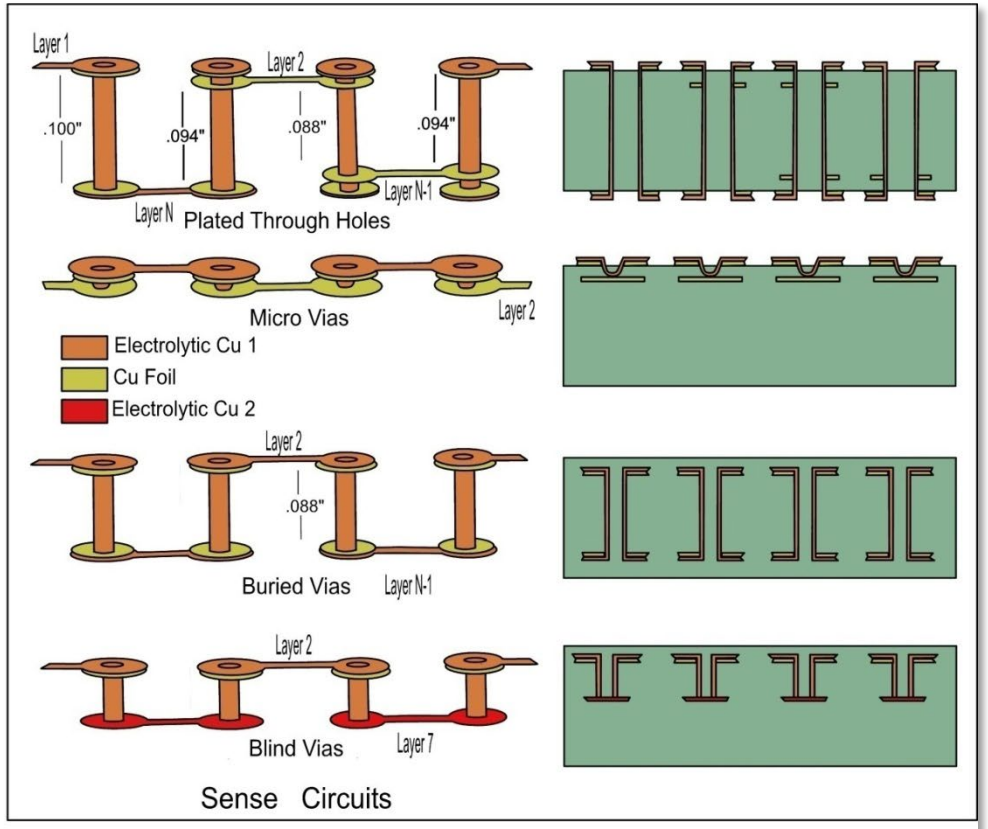
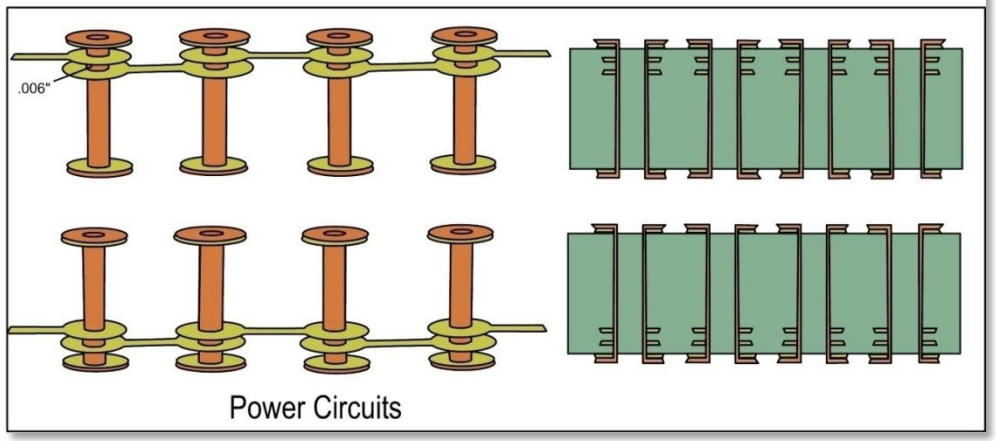
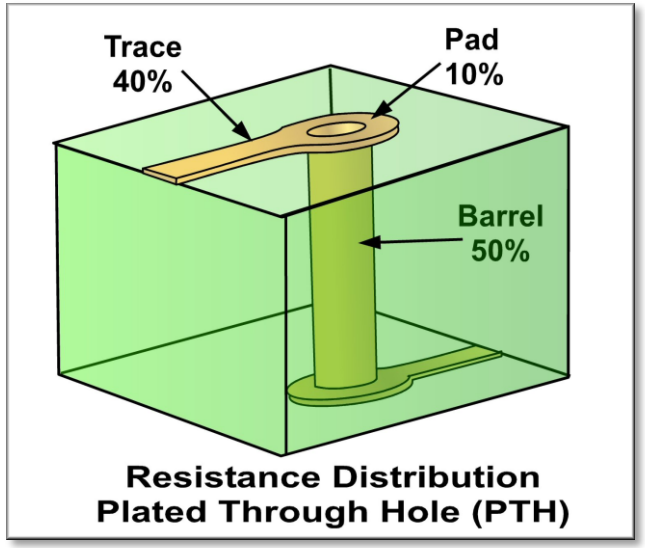
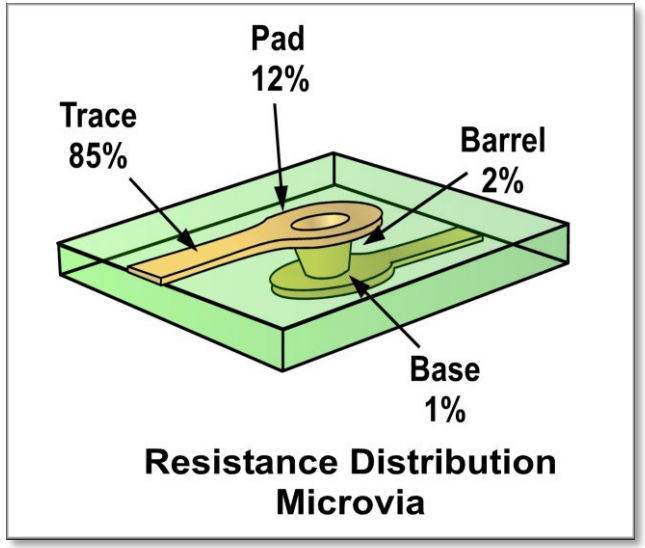


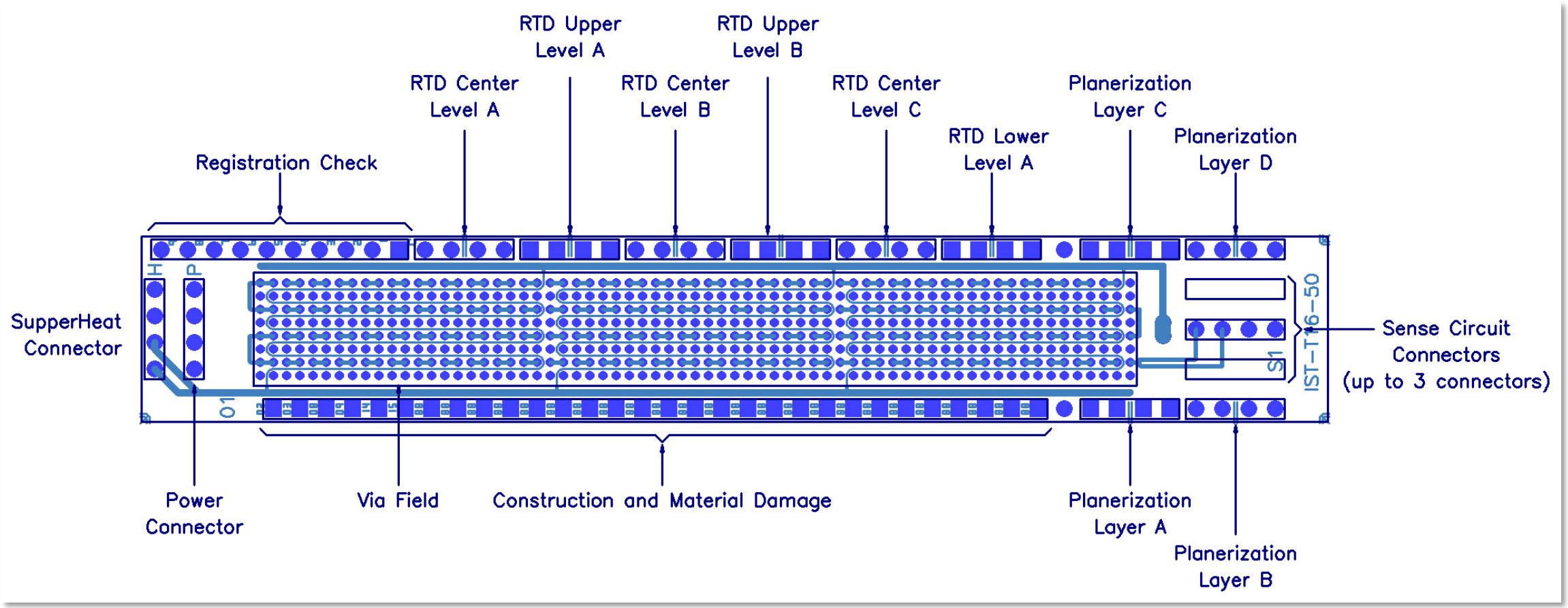


IST Testcoupon:



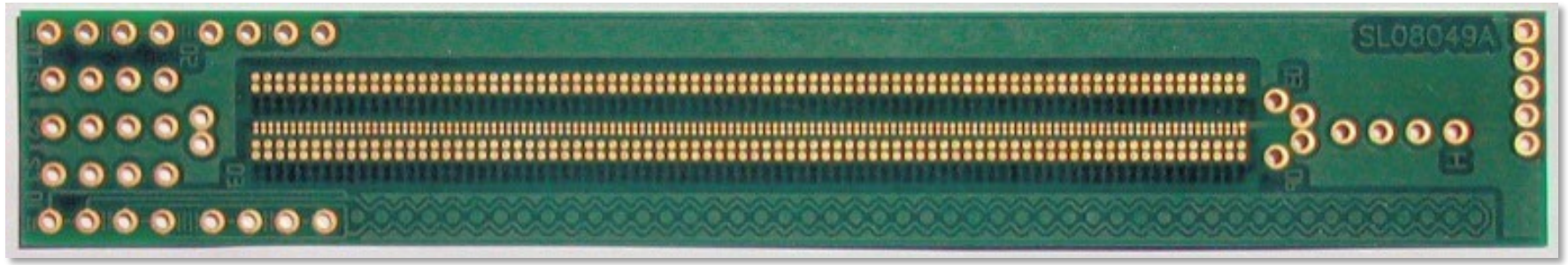


Coupons follow IST standard “X” design:



Heating Circuit(H) located on Layers 1 and N

Coupon Design Considerations:



- the coupon must reflect the critical attributes of the PWB
- the coupon thickness, layer count, copper weights, holes sizes, surface finish, grid size and construction are all established by the requirements of the customers design
- the line width is the one variable that is adjustable by the IST coupon designer. Line widths are adjusted to assure the
- resistance measurements on the power and sense circuit are optimized for maximum thermal and measurement efficiency

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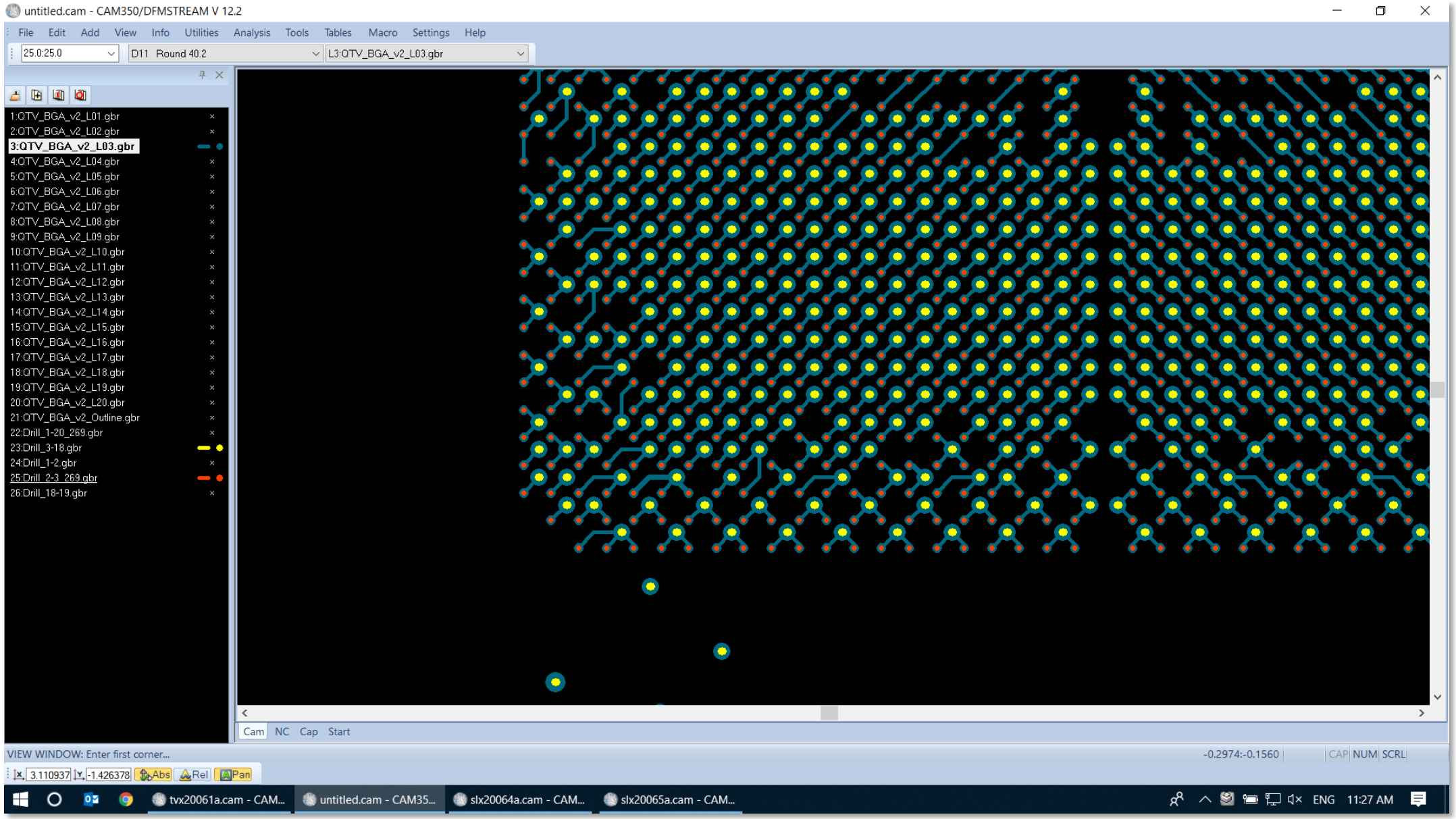
Replicating CAD design features:



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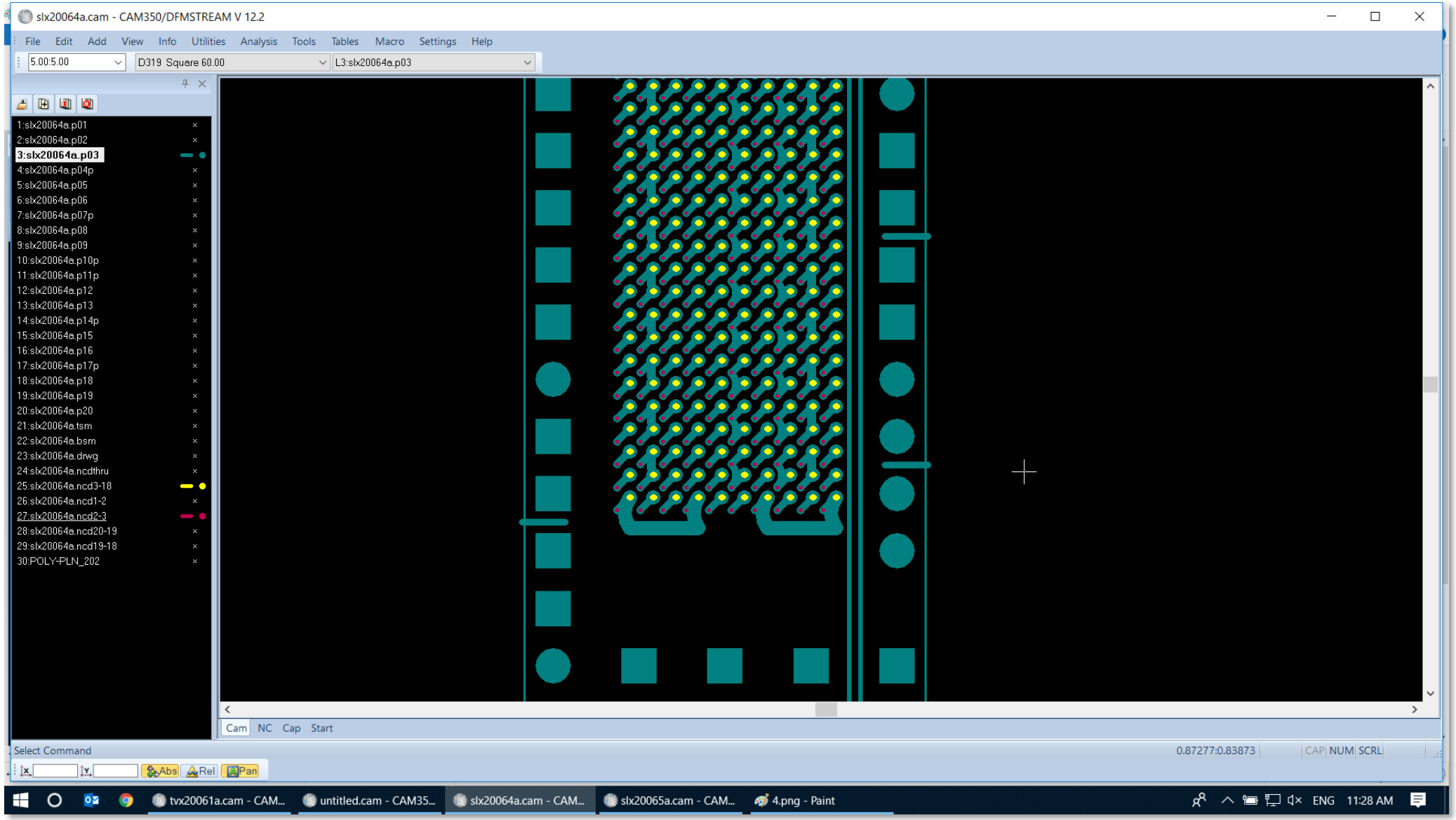
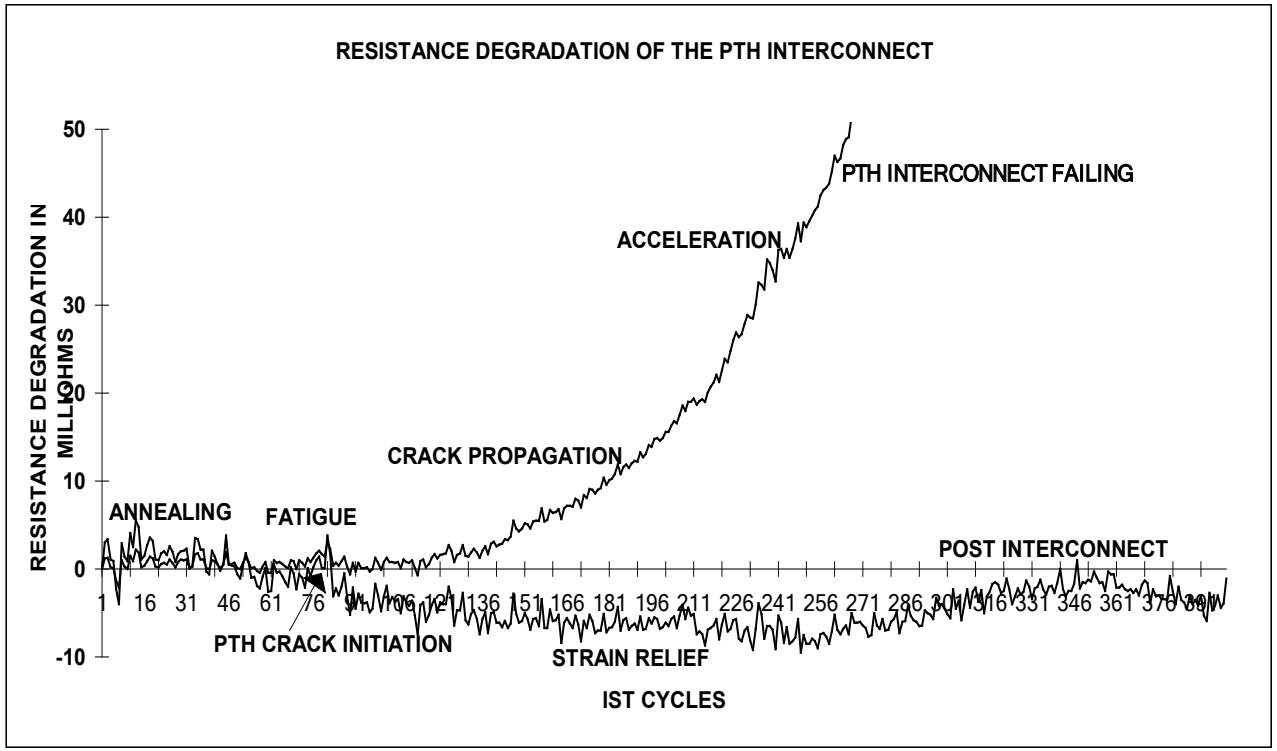
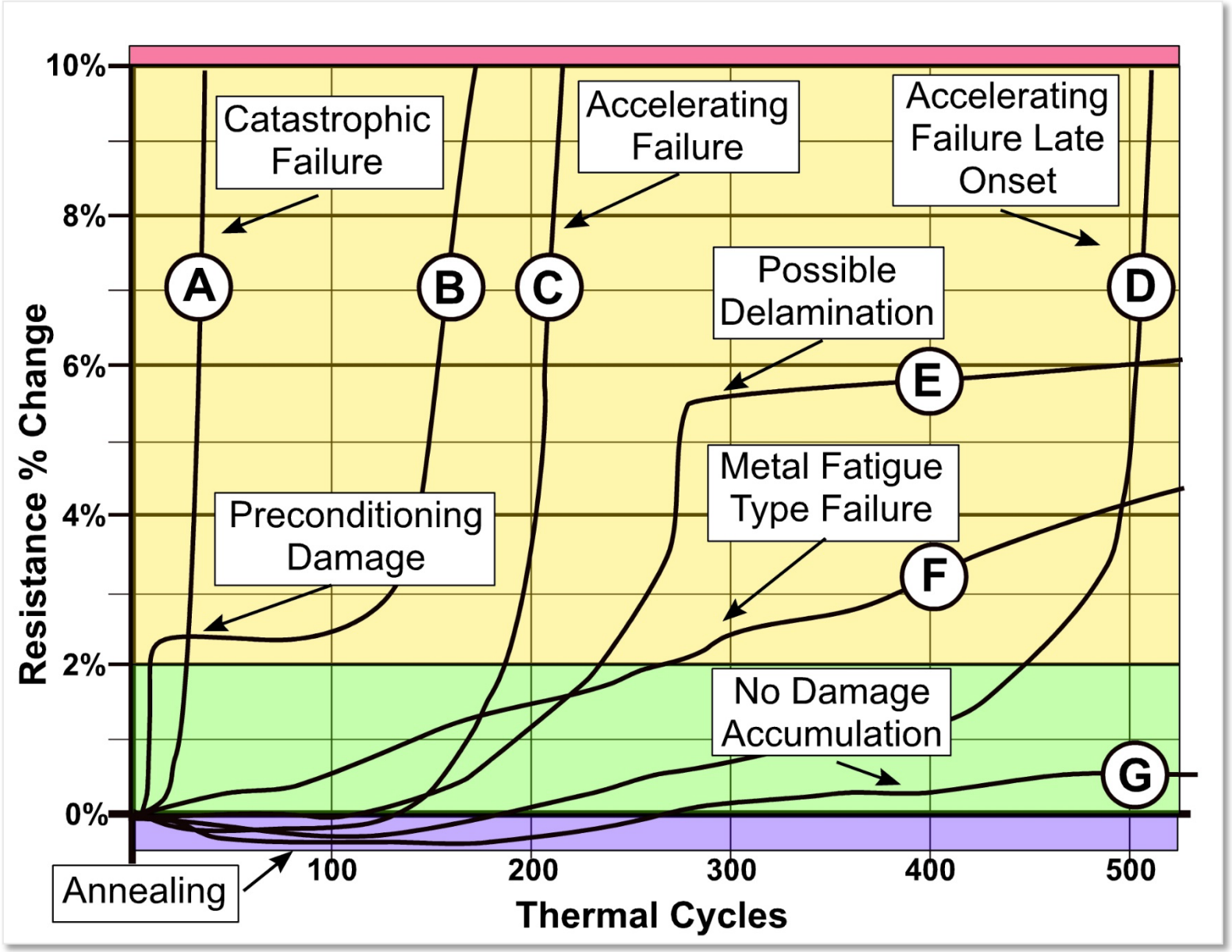
Replicated Feature in Coupon:



Resistance Degradation of the Interconnect:



IST Resistance Graph:



IST-HC System Hardware:

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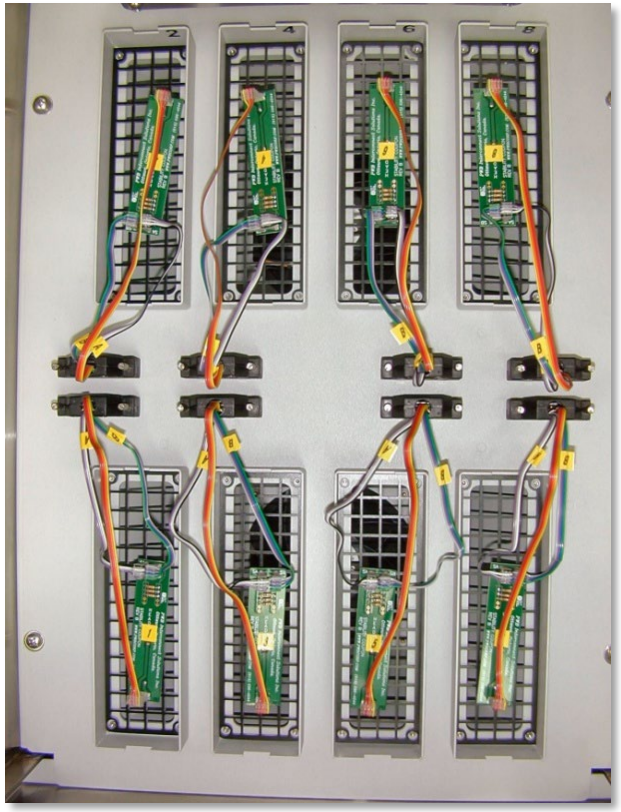
Number 2.6.26	
Subject: DC Current Induced Thermal Cycling Test	
Date: 11/99	Revision: Proposal
Originating Committee: Test Methods Subcommittee (7-11)	

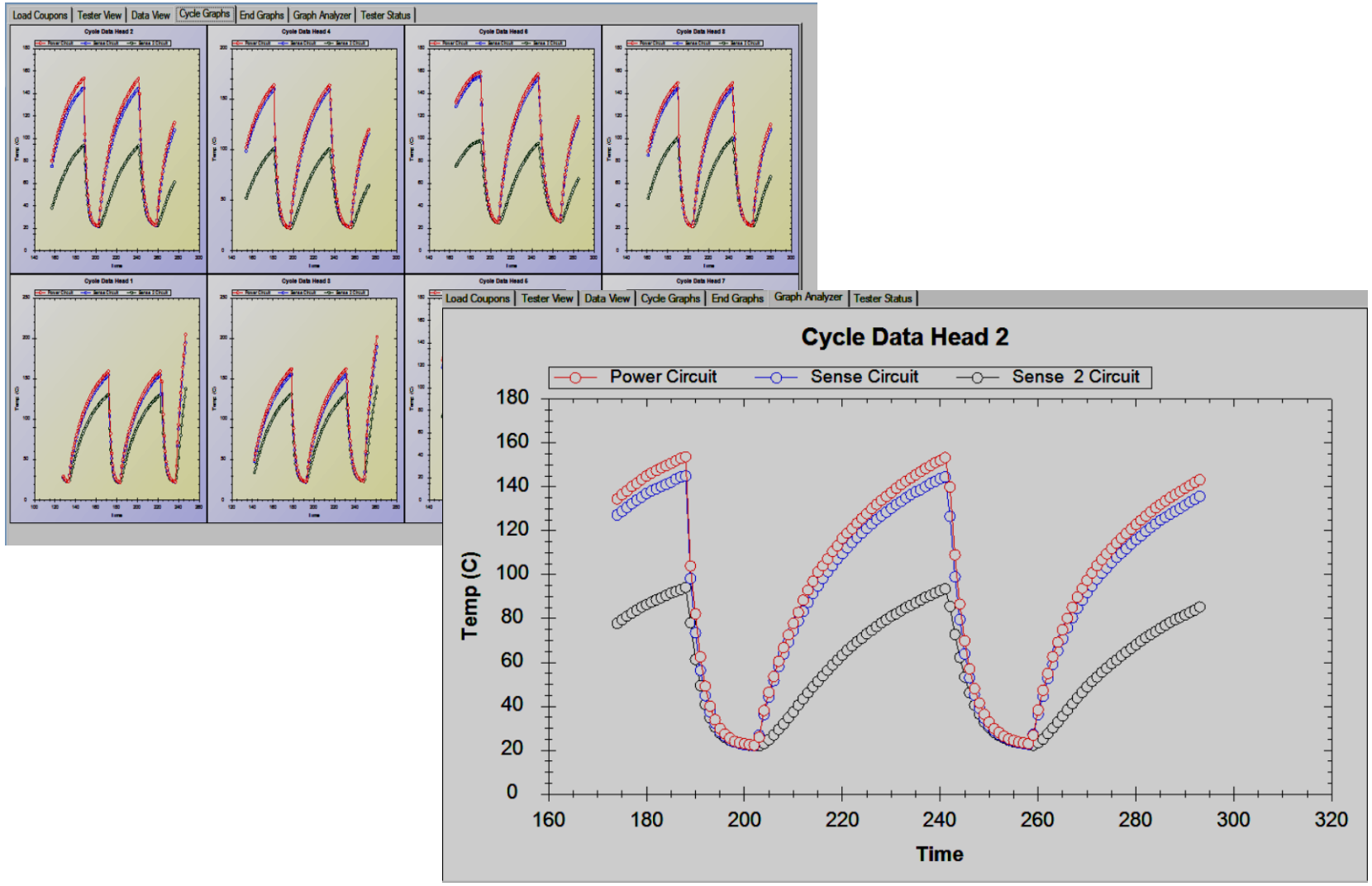
IPC-TM-650
Test Methods Manual



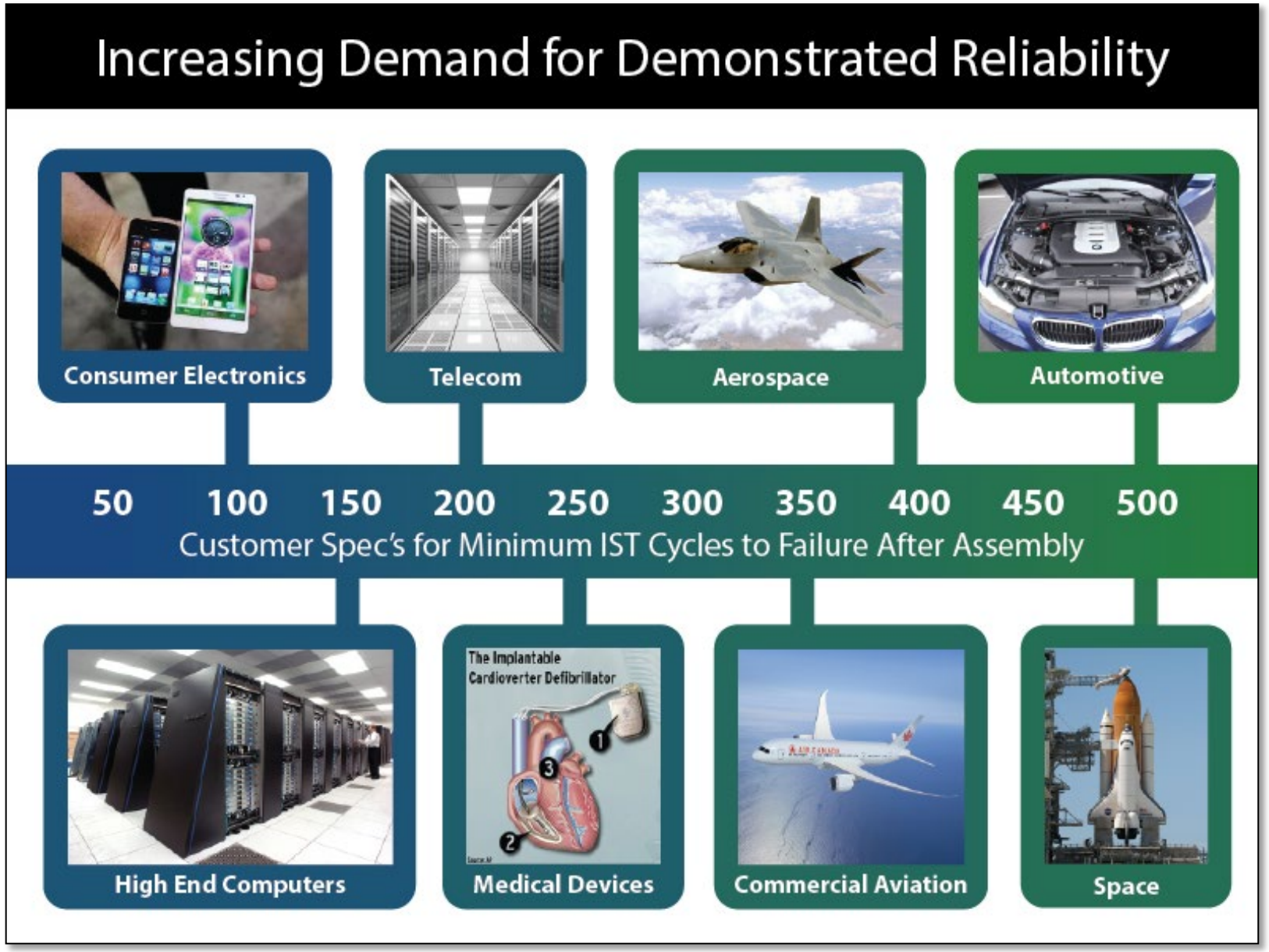
8 Coupon Bays

Coupon Data on 8 channels:

Temperature/Resistance recording on 8 heads :

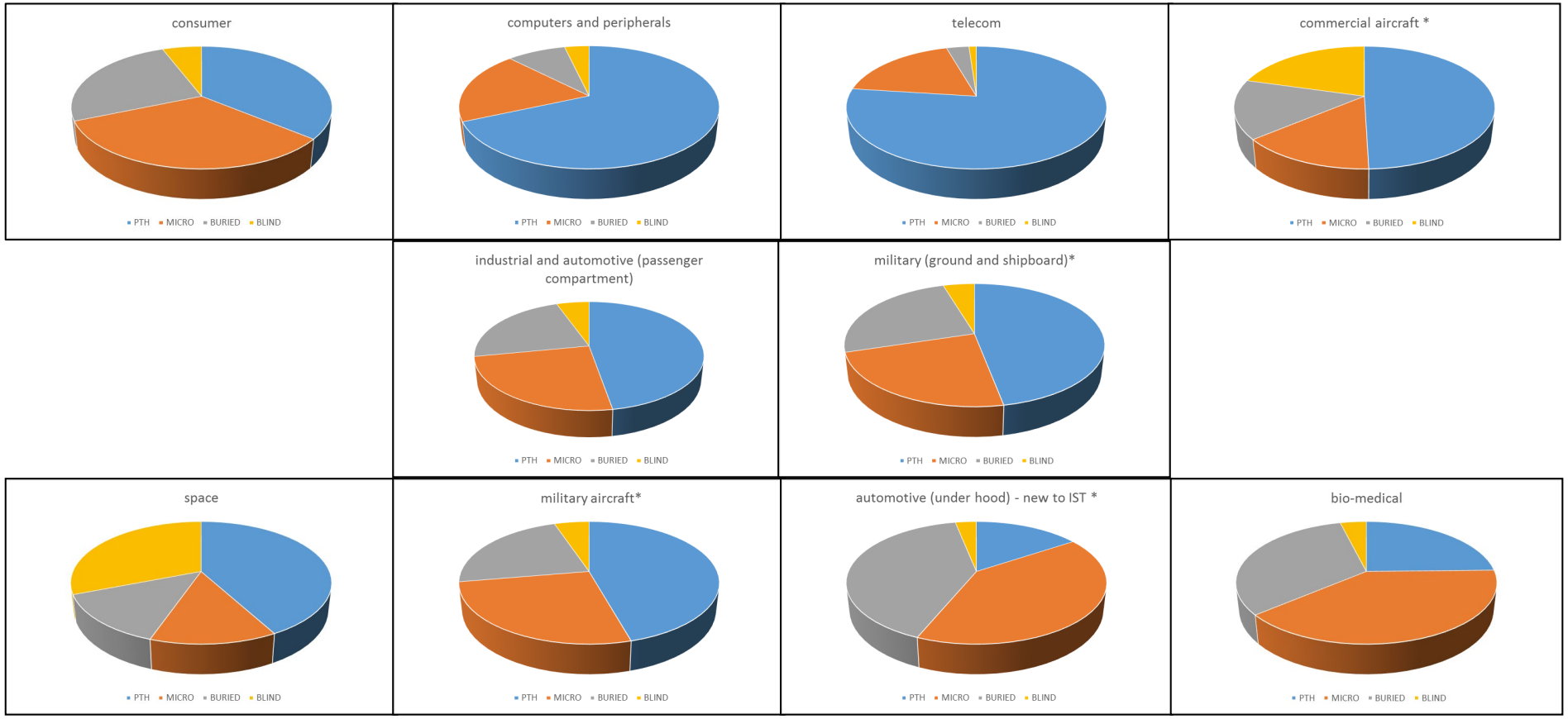


Typical IST cycle baseline according to application:



IST Via Structures By Industrial Segment:

Every industry is unique, common base-lining would be impossible



Every chart must then be further dissected by layer count, thickness, construction, hole size, material type, etc. to fully understand the levels of complexity involved.

Testing as per section 9.5.5 titled Interconnect Stress Testing (IST):

ECSS-Q-ST-70-60C – Interconnection stress testing (IST):

- Current-induced thermal cycling (IPC-TM-650-2.6.26 Method A) with continuous resistance monitoring of power and sense circuits
- All coupons Baked 8 Hours at 120 °C
- Test parameters
  - Six times preconditioning to 230 °C using “superheat” circuit applying IPC profile
  - Cycling from RT to 150 °C for mechanical vias (S1 and S3)
  - Cycling from RT to 190 °C for microvias (S2)
- Acceptance criteria for microvias
  - Less than 10 % increase in resistance for mechanical Vias
  - Less than 5 % increase in resistance for microvias
  - IST endurance of Max 500 cycles

Typical IST cycle baseline according to application:

Association Connecting Electronics Industries

IPC®

3000 Lakeside Drive, Suite 309S
Bannockburn, IL 60015-1249

IPC-TM-650
TEST METHODS MANUAL

Number	
2.6.26	
Subject	
DC Current Induced Thermal Cycling Test	
Date	Revision
5/14	**A**
Originating Task Group	
PTV Reliability Test Methods (6-10c)	

1 Scope These methods determine the physical endurance of representative coupons of printed boards to a series of high temperature excursions from ambient. The temperature excursions cause thermo-mechanical fatigue of the electrical interconnect structures.

The test coupon is resistance heated by passing DC current through the coupon to bring the temperature of the copper to a designated temperature. Switching the current on and off creates thermal cycles between room temperature and the designated temperature within the sample. The laminate and surrounding materials are heated to different extents depending on the thermal conductivity of the materials. The thermal cycling can accelerate latent interconnect anomalies to failure.

The number of cycles achieved permits a quantitative assessment of the performance.

1.1 Method A Description Method A uses a coupon with two or more independent electrical nets. The designation for these nets is either a power net (P) or a sense net (S). Each electrical net consists of plated barrels and conductors (internal and external). DC current is passed through one electrical net to heat the coupon to a designated temperature. When the electrical net is at the designated temperature, the DC current is turned off and cooling fans are turned on to cool the coupons to ambient temperature. One heating and cooling sequence represents a thermal cycle. Thermal cycling is continued to either a set number of cycles or a failure. Temperature coefficient of resistance (TCR) is estimated by proprietary algorithms.

A failure is based on a percentage change in the bulk resistance of the coupon at the designated test temperature. The percentage change is measured independently for each electrical net being tested. When the percentage change is exceeded, the test is stopped for the coupon.

1.2 Method B Description Method B uses a coupon with one electrical net. The net consists of via structures connected by external and/or internal circuit lines in a daisy chain. DC current is passed through the electrical net to heat the coupon to a designated temperature. When the electrical net is at the designated temperature, the DC current is turned off and a cooling fan is turned on to cool the coupons to ambient temperature. One heating and cooling sequence represents a thermal cycle. Thermal cycling is continued to either a set number of cycles or a failure. Temperature coefficient of resistance (TCR) is measured.

A failure is based on a percentage change in the bulk resistance of the coupon at the designated test temperature. The percentage change is measured independently for each electrical net being tested. When the percentage change is exceeded, the test is stopped for the coupon.

2 Applicable Documents

2.1 IPC[1]

IPC-MDP-650 Method Development Packet

IPC-TM-650 Test Methods Manual[2]

2.1.1 Microsectioning

2.5.35 Capacitance of Printed Board Substrates After Exposure to Assembly, Rework, and/or Reliability Tests. (At the time of publication of this test method, 2.5.35 is in development.)

2.6.27 Thermal Stress, Convection Reflow Assembly Simulation

3 Test Specimens A typical daisy chain test coupon for each method is shown in Figure 3-1 and Figure 3-2.

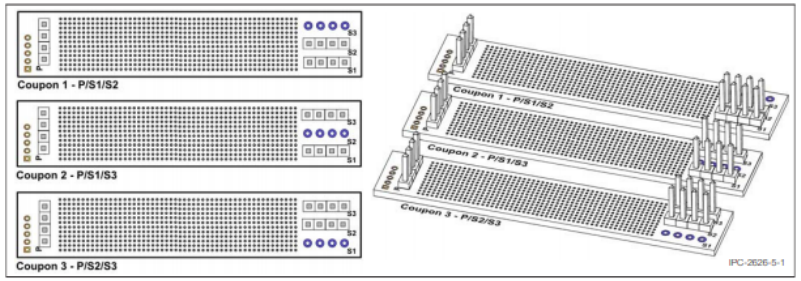


Figure 5-1 Examples of Three Dual Sense IST Test Coupons *(Top-Down View as shown at left and Isometric View as shown at right)*

5.2.2 Position the coupons at each test head by attaching male to female connectors.

5.2.3 Baseline Performance (Optional) Establish a performance baseline by completing two Method A cycles and then stop the test at the end of the cooling cycle.

5.2.4 Capacitance Test (Optional) If required, the capacitance test **shall** be performed per IPC-TM-650, Method 2.5.35.

5.2.5 Assembly Precondition (Optional) Assembly preconditioning is recommended to simulate the assembly environment to which the printed boards are exposed (see 6.1).

5.2.6 Unless otherwise specified by the user, test all via types and materials per the default test condition in accordance with Table 5-1. For testing of samples containing microvia structures, use the microvia test condition. For testing of samples containing polyimide materials, use the polyimide test condition.

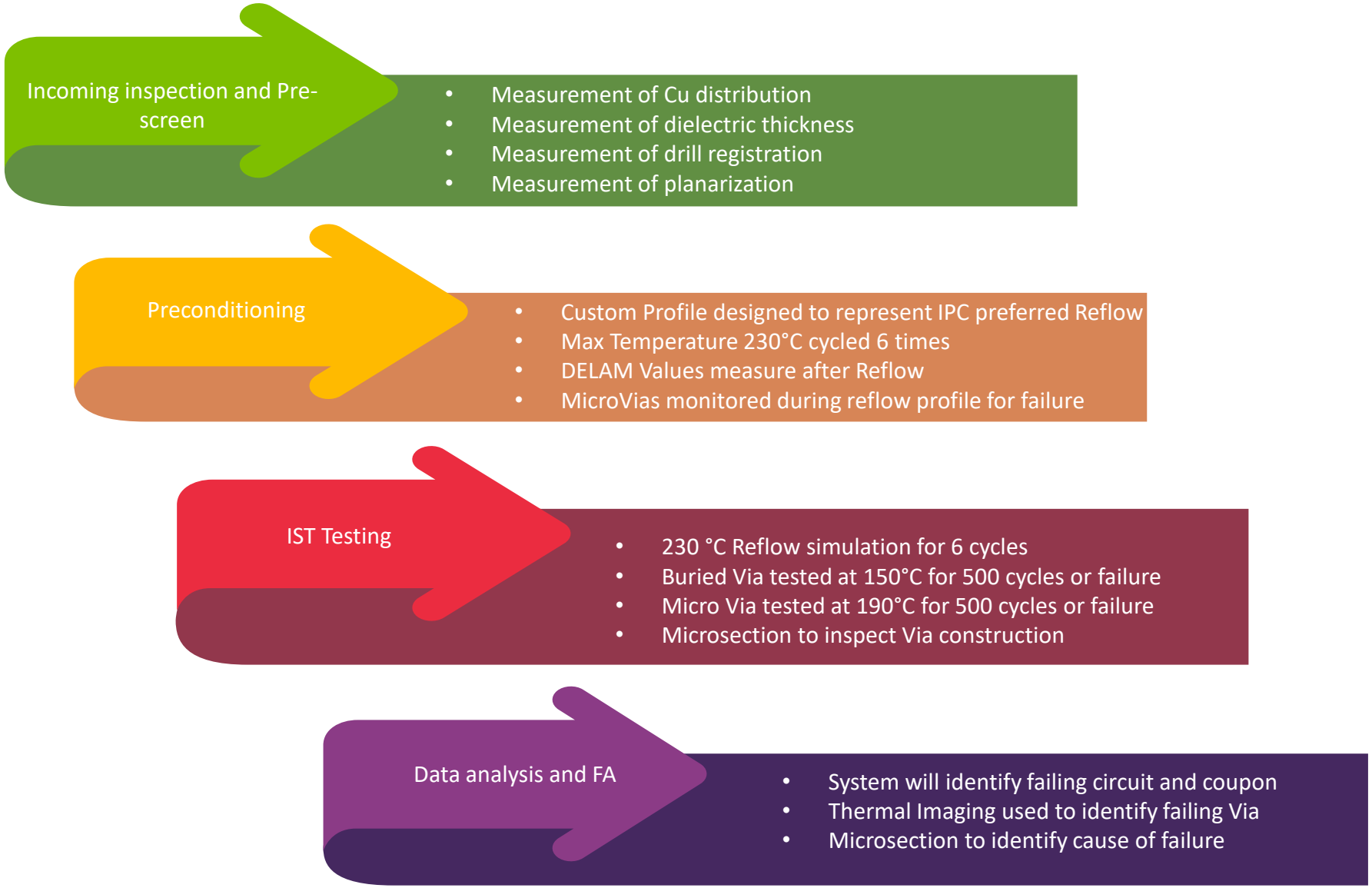
5.2.7 Pre-Cycling Test Sequence The following paragraphs detail the sequence for a single coupon, however this sequence is done at all test heads simultaneously. The ambient resistance, resistance at test temperature, rejection resistance, and current are calculated for each coupon and displayed on the PC monitor.

Table 5-1 Method A Typical Test Conditions

Test Condition	Number of Samples	Test Temperatures	Failure Threshold (Resistance Change)[1]	Number of Cycles	Data Collection Frequency (Cycles)	Precycle Time Window (seconds)	Compensation
Default	6	150 °C	10%	250	25	3	Calculated
Polyimide	6	AABUS	10%	250	25	3	Calculated
Microvias[2]	6	190 °C	10%	250	25	3	None
Polyimide Microvias[2]	6	AABUS	10%	250	25	5	None
Survivability Testing	6	230 °C	10%	10	1	5	None
	6	245 °C	10%	10	1	5	None
	6	260 °C	10%	10	1	5	None

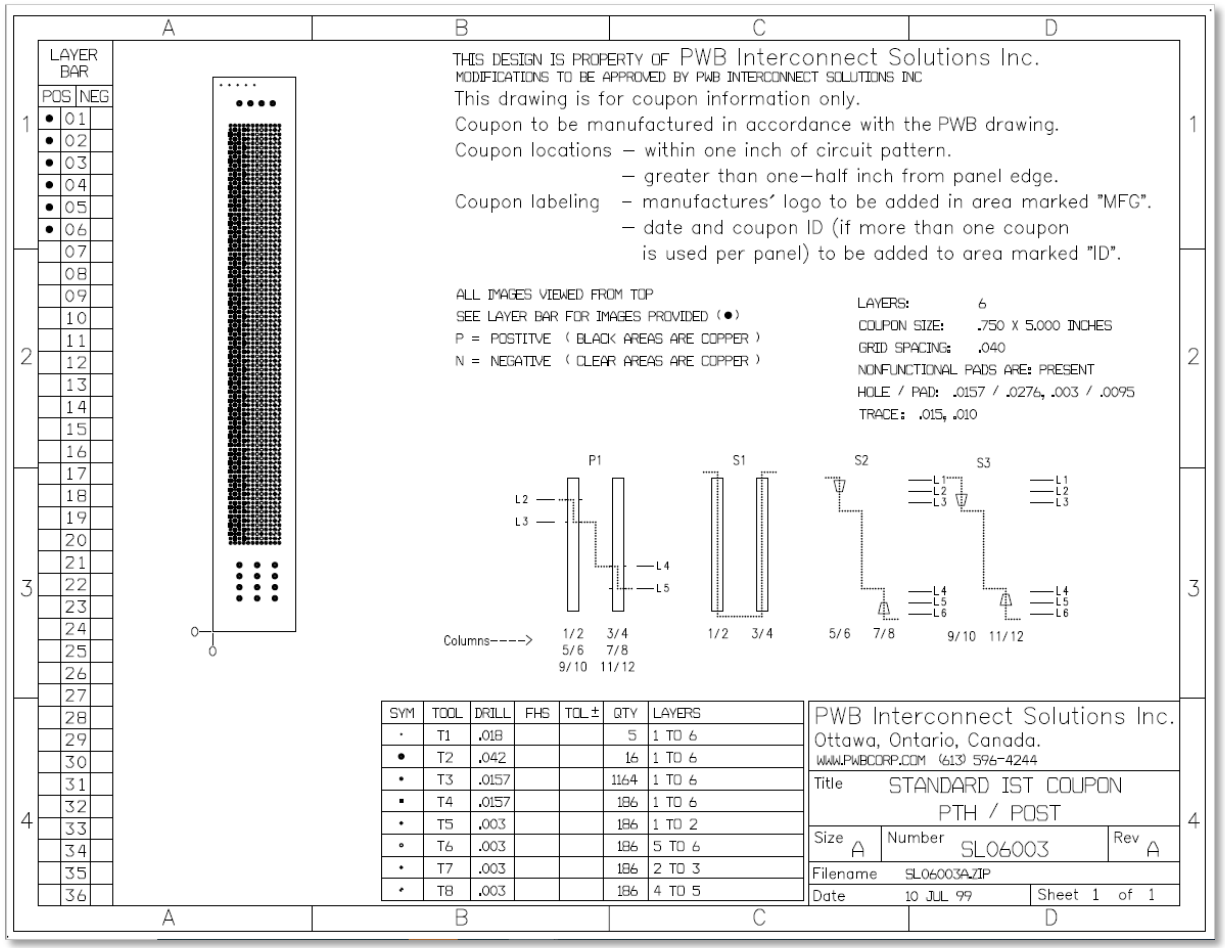
Note 1. For Dual Sense Testing, both the "Cycle Using" and the "Cycle Failing On" fields on the Method A test equipment **shall** be set to 'both sense circuits.'
Note 2. Power on the microvia or heating trace net.

PWBi – IST Key Deliverables:



Microvia testing using IST:

First IST micro Via design in 1999



LAYER BAR

POS	NEG
● 01	
● 02	
● 03	
● 04	
● 05	
● 06	
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THIS DESIGN IS PROPERTY OF PWB Interconnect Solutions Inc.
MODIFICATIONS TO BE APPROVED BY PWB INTERCONNECT SOLUTIONS INC

This drawing is for coupon information only.
Coupon to be manufactured in accordance with the PWB drawing.
Coupon locations – within one inch of circuit pattern.
– greater than one–half inch from panel edge.
Coupon labeling – manufactures' logo to be added in area marked "MFG".
– date and coupon ID (if more than one coupon is used per panel) to be added to area marked "ID".

ALL IMAGES VIEWED FROM TOP
SEE LAYER BAR FOR IMAGES PROVIDED (●)
P = POSITIVE (BLACK AREAS ARE COPPER)
N = NEGATIVE (CLEAR AREAS ARE COPPER)

LAYERS: 6
COUPON SIZE: .750 X 5.000 INCHES
GRID SPACING: .040
NONFUNCTIONAL PADS ARE: PRESENT
HOLE / PAD: .0157 / .0276, .003 / .0095
TRACE: .015, .010

P1 S1 S2 S3

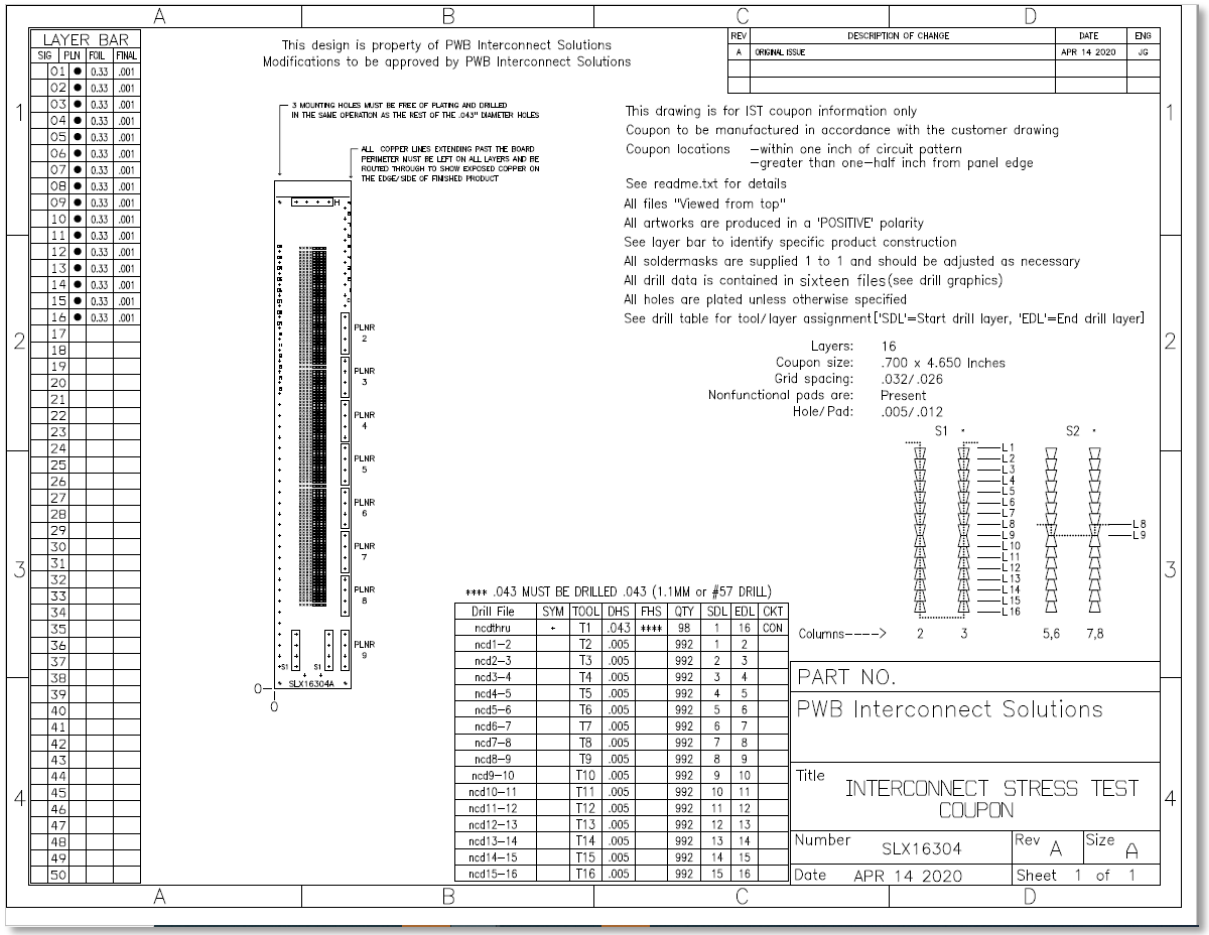
Columns----> 1/2 5/6 9/10 11/12 | 1/2 3/4 | 5/6 7/8 | 9/10 11/12

SYM	TOOL	DRILL	FHS	TOL ±	QTY	LAYERS
·	T1	.018			5	1 TO 6
●	T2	.042			16	1 TO 6
•	T3	.0157			1164	1 TO 6
▪	T4	.0157			186	1 TO 6
•	T5	.003			186	1 TO 2
◦	T6	.003			186	5 TO 6
•	T7	.003			186	2 TO 3
•	T8	.003			186	4 TO 5

PWB Interconnect Solutions Inc.
Ottawa, Ontario, Canada.
WWW.PWBCORP.COM (613) 596-4244

Title: STANDARD IST COUPON PTH / POST
Size: A | Number: SL06003 | Rev: A
Filename: SL06003AZIP
Date: 10 JUL 99 | Sheet 1 of 1

Current Consumer Type design released 2020



LAYER BAR

SIG	PLN	FOIL	FINAL
01	●	0.33	.001
02	●	0.33	.001
03	●	0.33	.001
04	●	0.33	.001
05	●	0.33	.001
06	●	0.33	.001
07	●	0.33	.001
08	●	0.33	.001
09	●	0.33	.001
10	●	0.33	.001
11	●	0.33	.001
12	●	0.33	.001
13	●	0.33	.001
14	●	0.33	.001
15	●	0.33	.001
16	●	0.33	.001
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This design is property of PWB Interconnect Solutions
Modifications to be approved by PWB Interconnect Solutions

REV	DESCRIPTION OF CHANGE	DATE	ENG
A	ORIGINAL ISSUE	APR 14 2020	JG

3 MOUNTING HOLES MUST BE FREE OF PLATING AND DRILLED IN THE SAME OPERATION AS THE REST OF THE .043" DIAMETER HOLES

ALL COPPER LINES EXTENDING PAST THE BOARD PERIMETER MUST BE LEFT ON ALL LAYERS AND BE ROUTED THROUGH TO SHOW EXPOSED COPPER ON THE EDGE/SIDE OF FINISHED PRODUCT

PLNR 2 PLNR 3 PLNR 4 PLNR 5 PLNR 6 PLNR 7 PLNR 8 PLNR 9

SLX16304A

This drawing is for IST coupon information only
Coupon to be manufactured in accordance with the customer drawing
Coupon locations –within one inch of circuit pattern
–greater than one–half inch from panel edge
See readme.txt for details
All files "Viewed from top"
All artworks are produced in a 'POSITIVE' polarity
See layer bar to identify specific product construction
All soldermasks are supplied 1 to 1 and should be adjusted as necessary
All drill data is contained in sixteen files(see drill graphics)
All holes are plated unless otherwise specified
See drill table for tool/layer assignment['SDL'=Start drill layer, 'EDL'=End drill layer]

Layers: 16
Coupon size: .700 x 4.650 Inches
Grid spacing: .032/.026
Nonfunctional pads are: Present
Hole/Pad: .005/.012

S1 S2

Columns----> 2 3 | 5,6 7,8

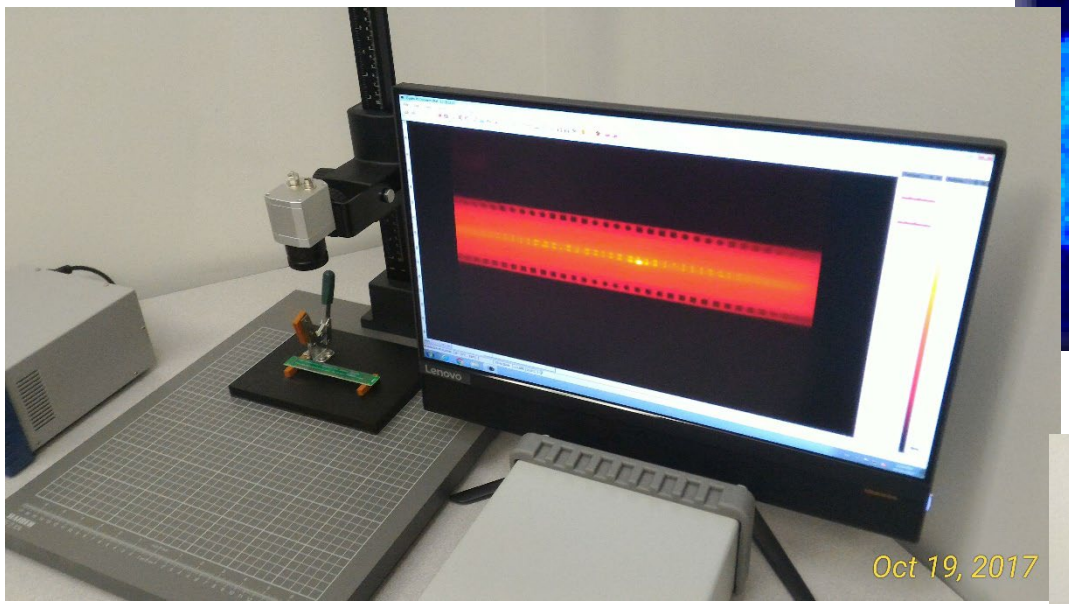
**** .043 MUST BE DRILLED .043 (1.1MM or #57 DRILL)

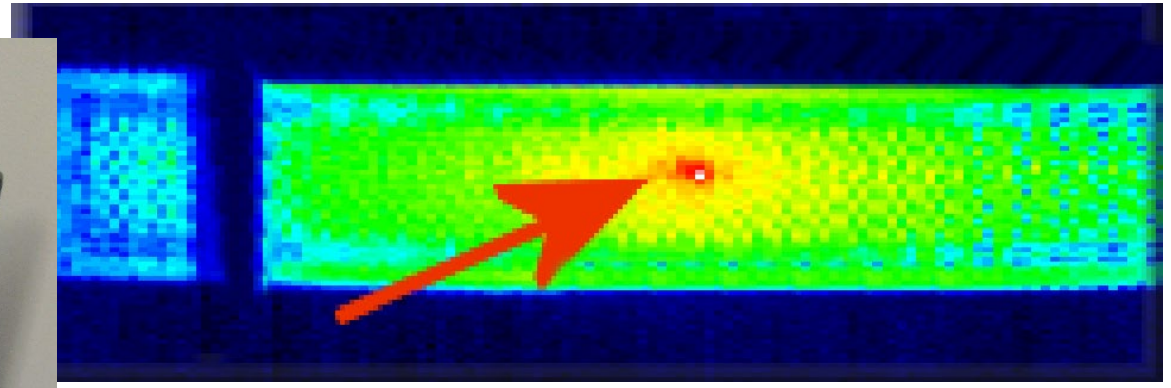
Drill File	SYM	TOOL	DHS	FHS	QTY	SDL	EDL	CKT
ncdthru	·	T1	.043	****	98	1	16	CON
ncd1–2		T2	.005		992	1	2	
ncd2–3		T3	.005		992	2	3	
ncd3–4		T4	.005		992	3	4	
ncd4–5		T5	.005		992	4	5	
ncd5–6		T6	.005		992	5	6	
ncd6–7		T7	.005		992	6	7	
ncd7–8		T8	.005		992	7	8	
ncd8–9		T9	.005		992	8	9	
ncd9–10		T10	.005		992	9	10	
ncd10–11		T11	.005		992	10	11	
ncd11–12		T12	.005		992	11	12	
ncd12–13		T13	.005		992	12	13	
ncd13–14		T14	.005		992	13	14	
ncd14–15		T15	.005		992	14	15	
ncd15–16		T16	.005		992	15	16	

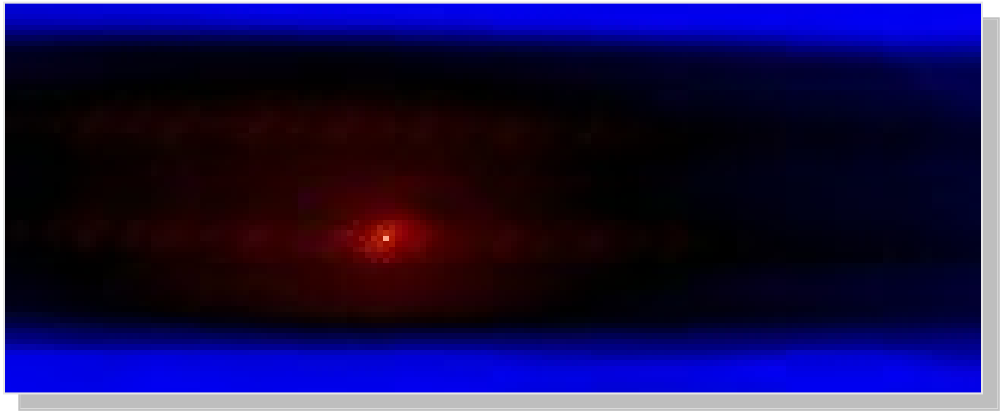
PART NO.
PWB Interconnect Solutions

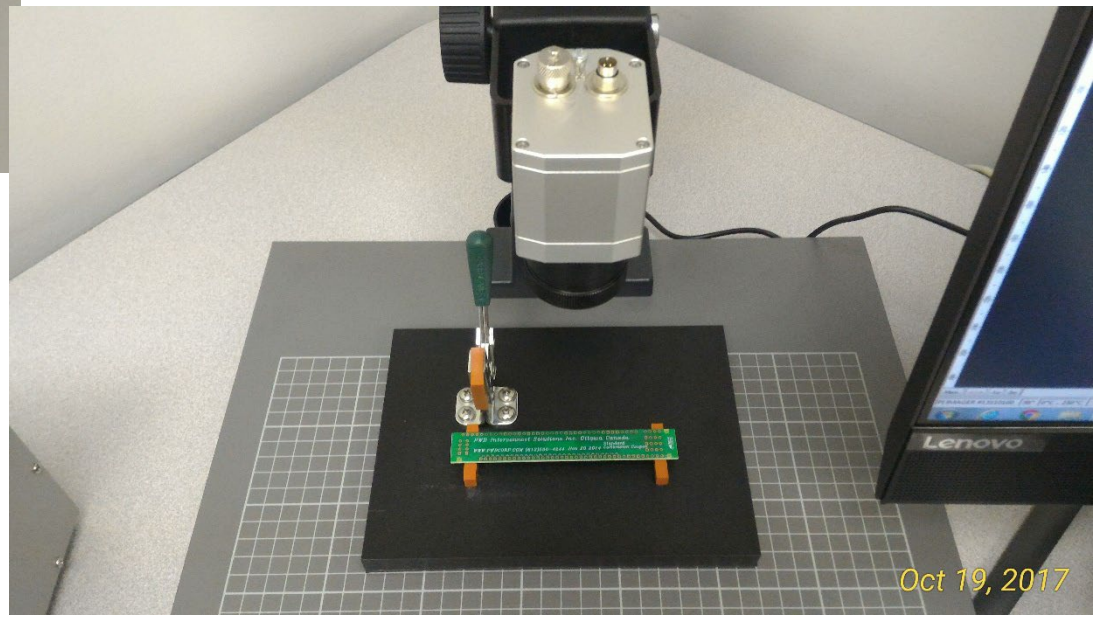
Title: INTERCONNECT STRESS TEST COUPON
Number: SLX16304 | Rev: A | Size: A
Date: APR 14 2020 | Sheet 1 of 1

Failure Identification using Infrared Camera:

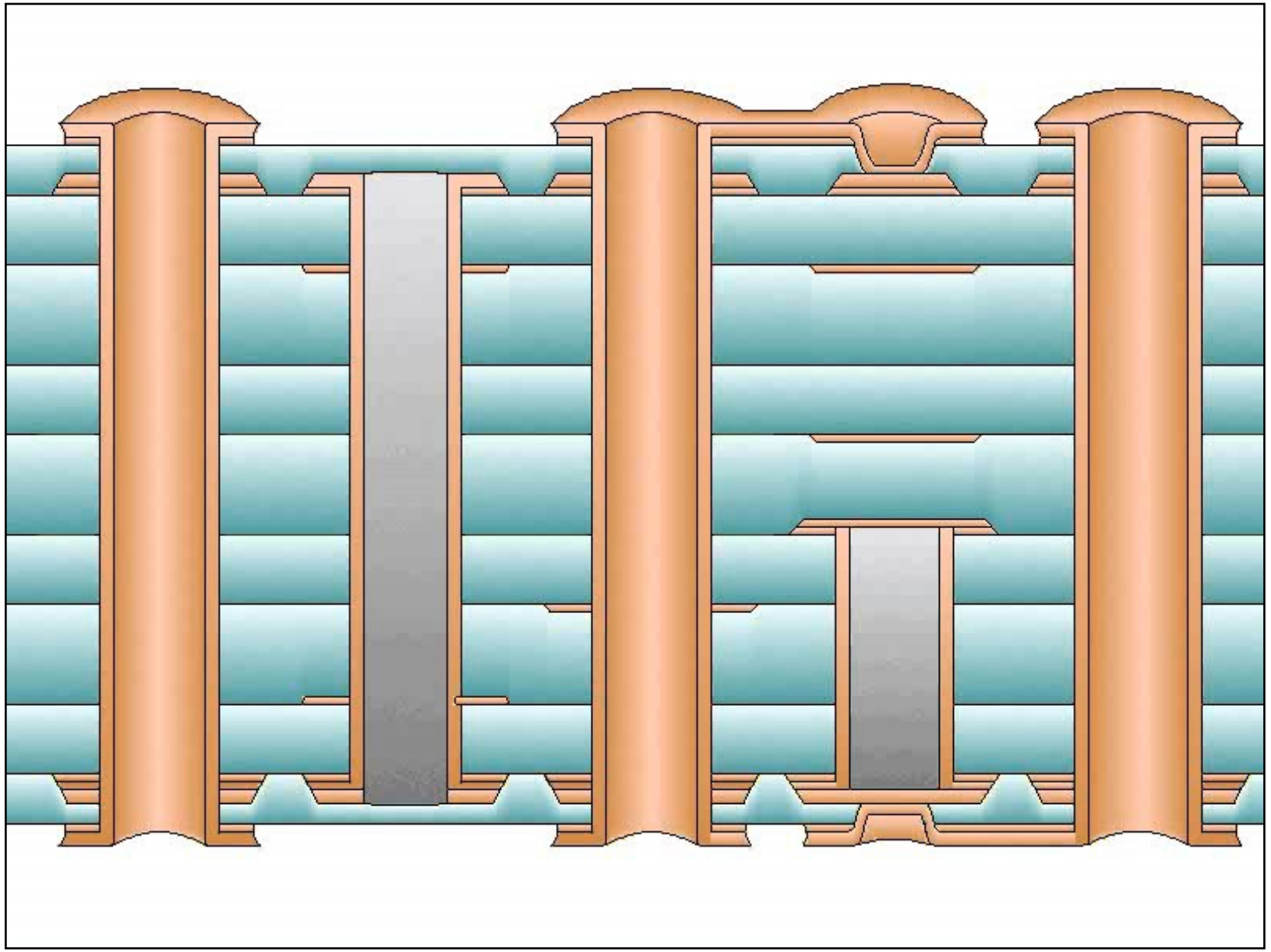




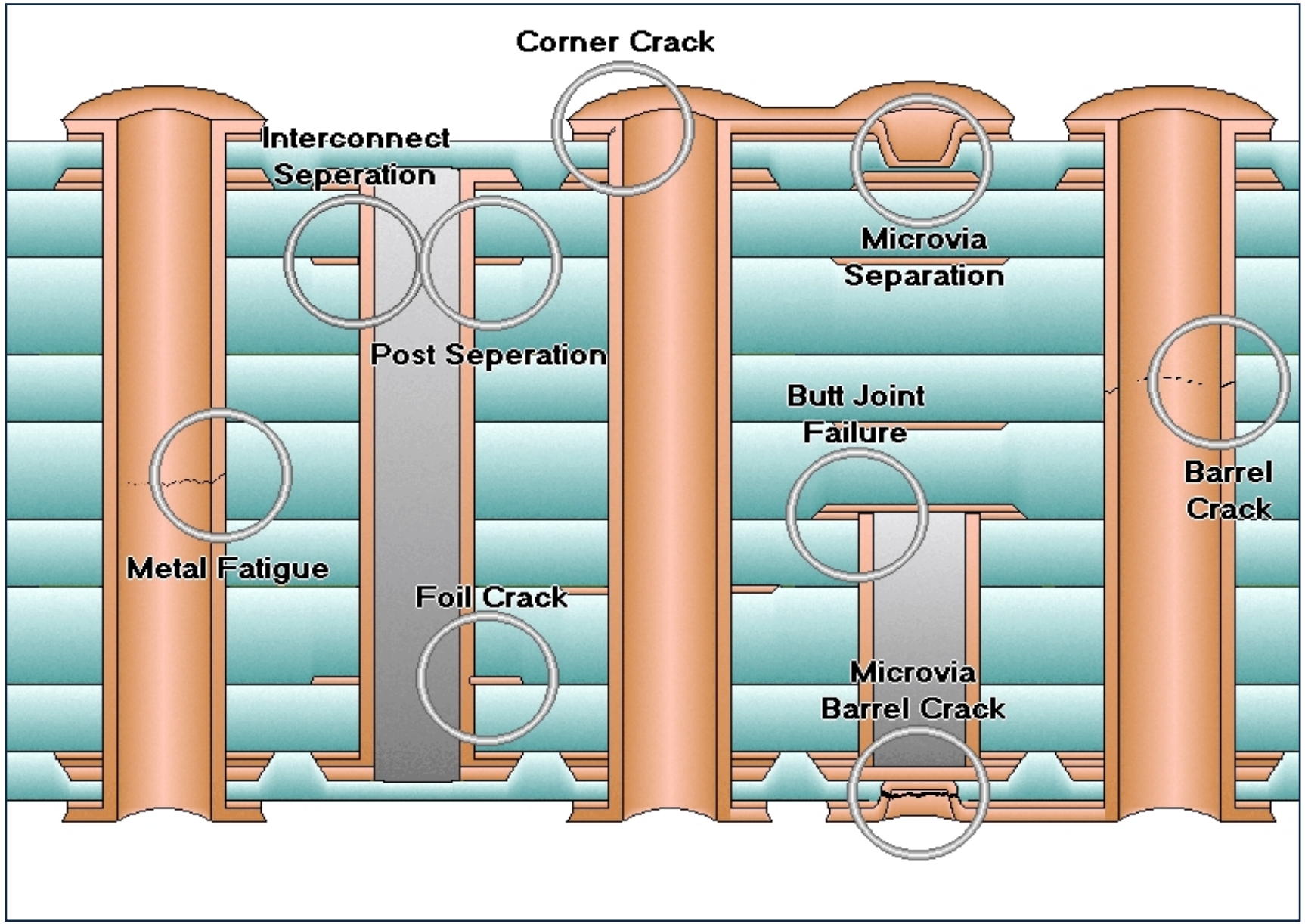




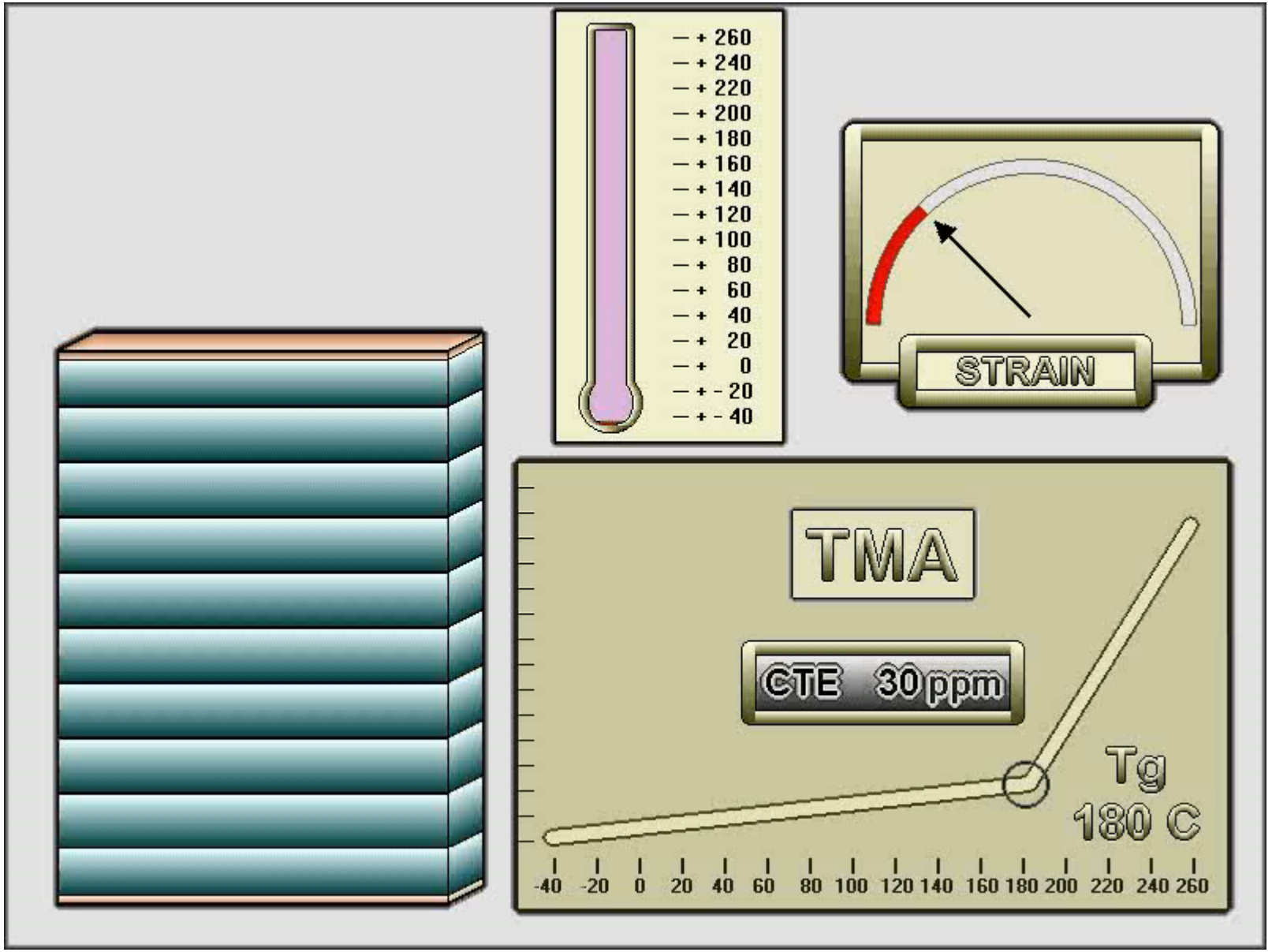
Thermal excursions in PCB:



PCB Failure Modes:



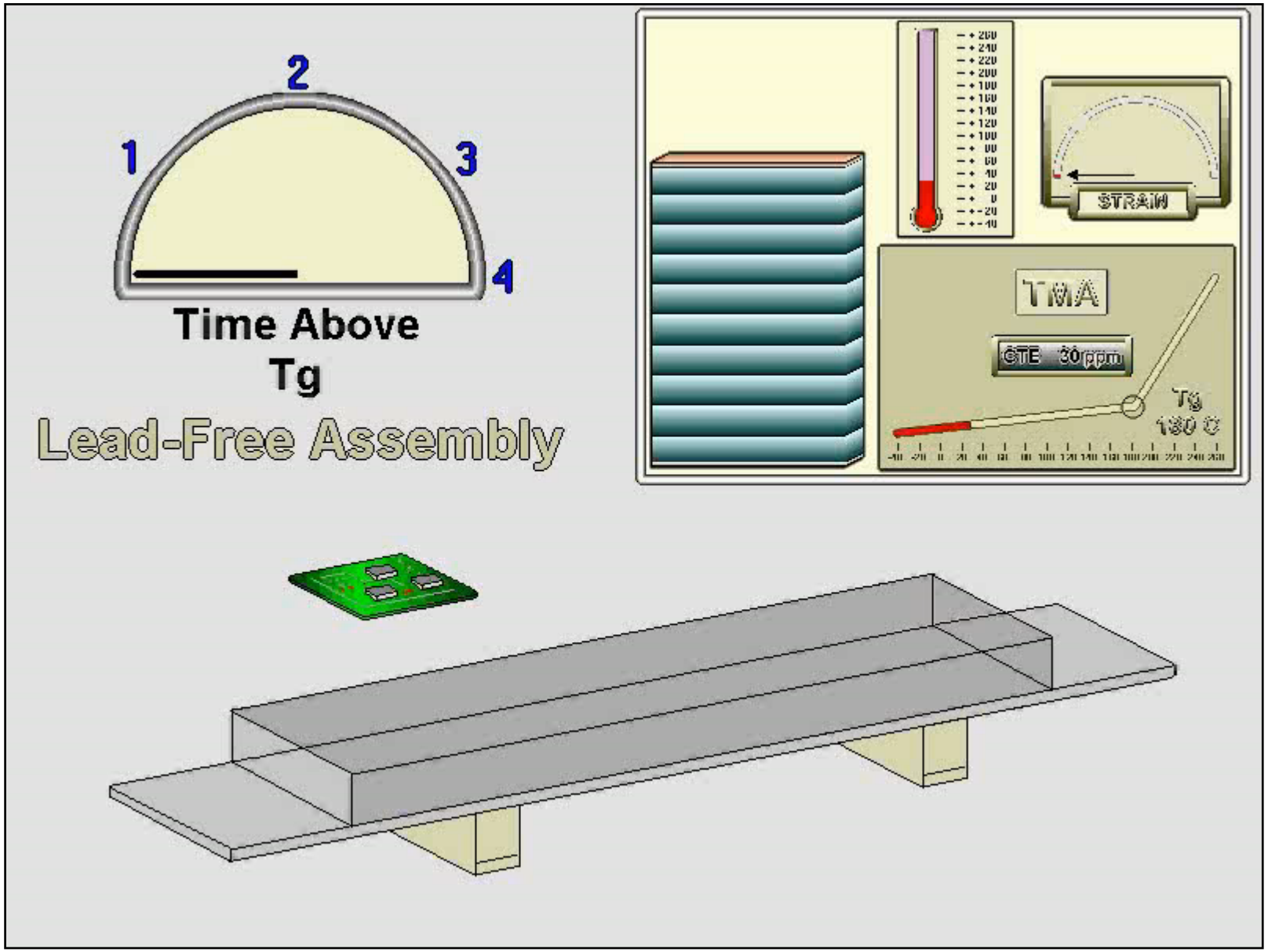
Thermal Expansion:



Base material shows a significant increase in thermal expansion at temperatures above Tg.

Copper expands at lower CTE compared to base material – this causes mechanical stress in the PCB stackup.

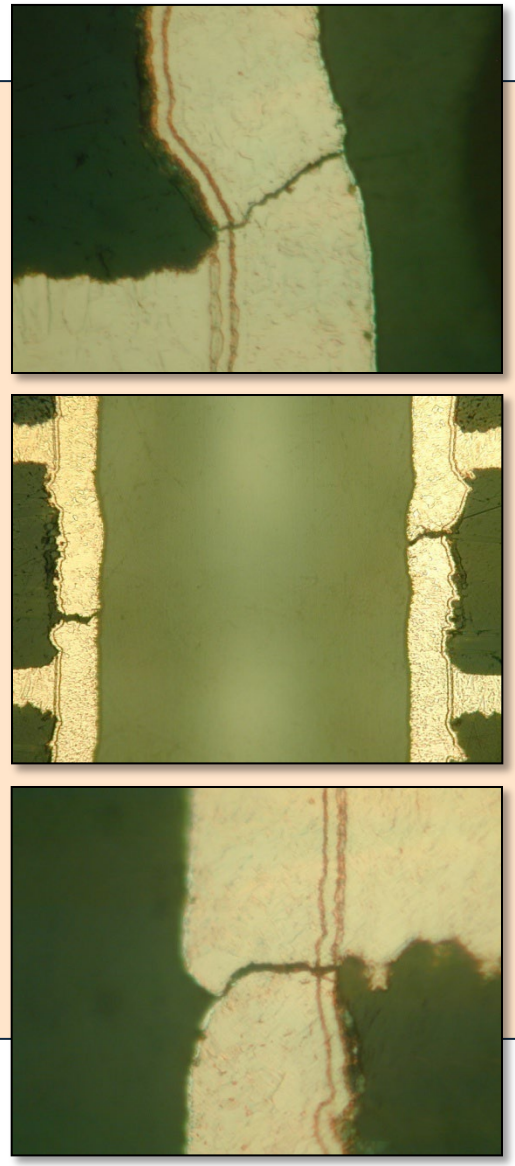
Lead Free Soldering Process:



Damage during the soldering process reduces the life expectancy of a PCB by approximately 50%.

The amount of damage depends on the time duration, the PCB is exposed to temperatures above Tg.

Microsections – Barrel Cracks:



- Barrel is stressed longitudinal

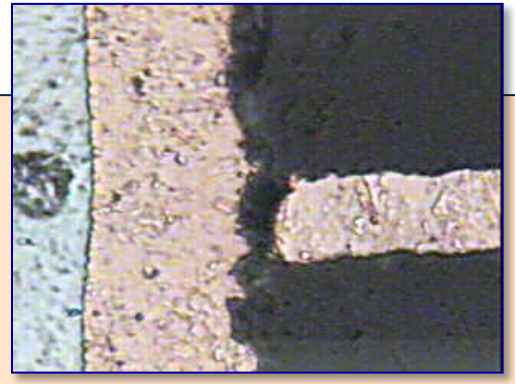
- Crack in side wall of barrel

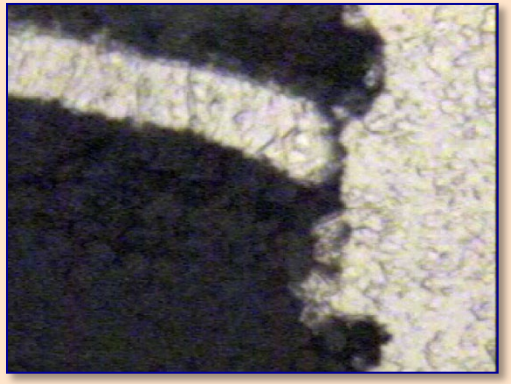
- fast damage progress

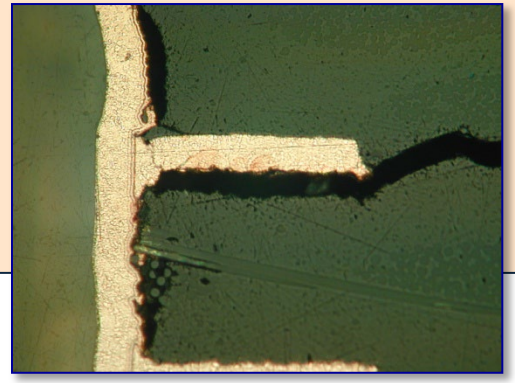
- usually large crack width

- interrupted at room temperature

Typical Post Separation Failure Modes:





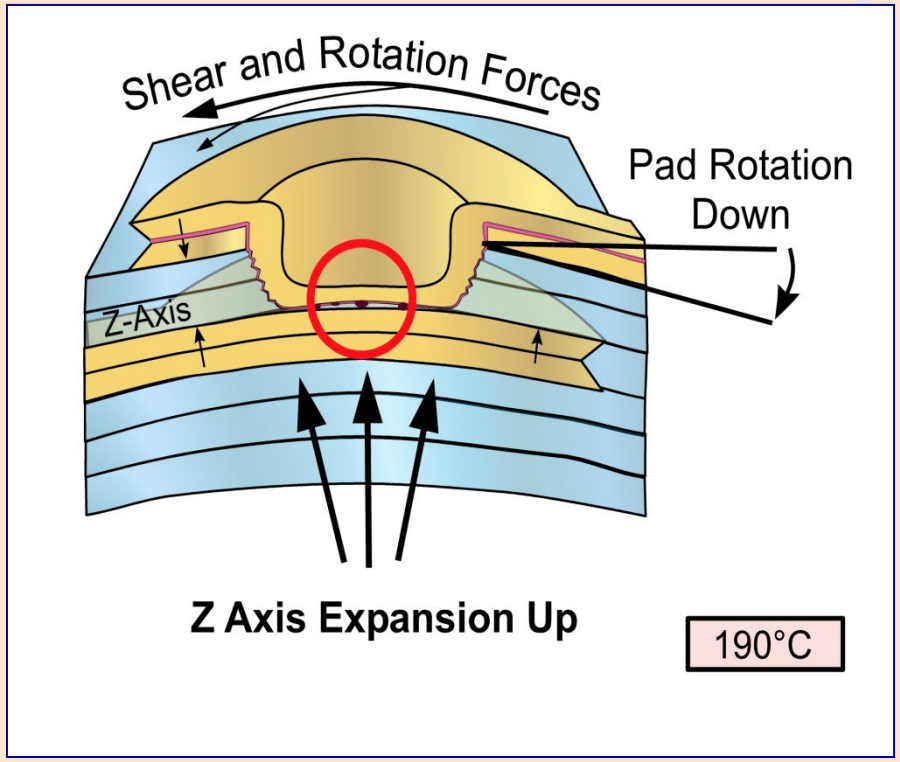


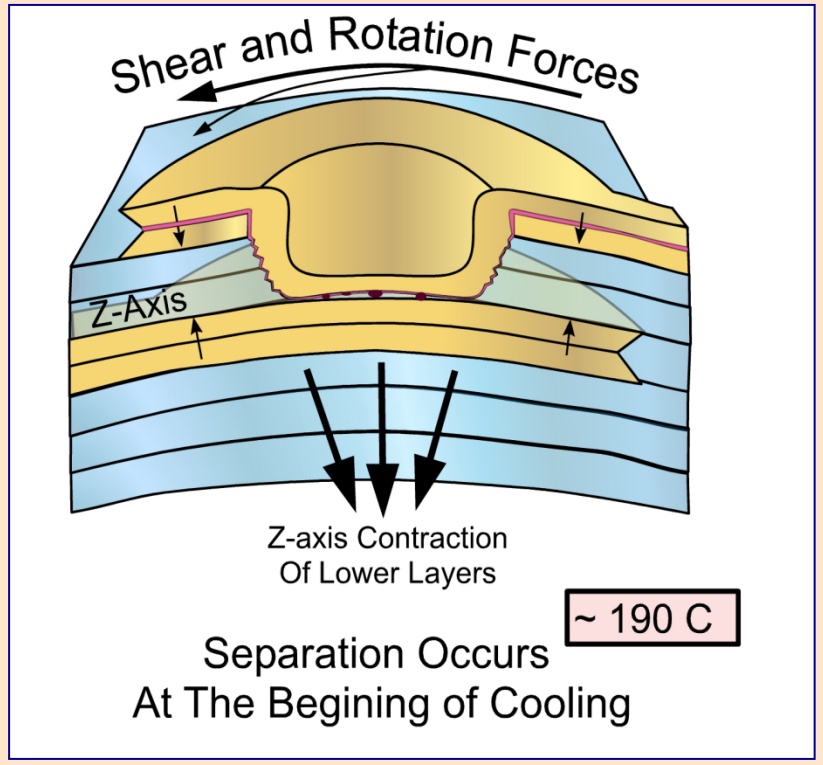
- fast damage progress

- usually large crack width

- interrupted at room temperature

Microvia-Separation:

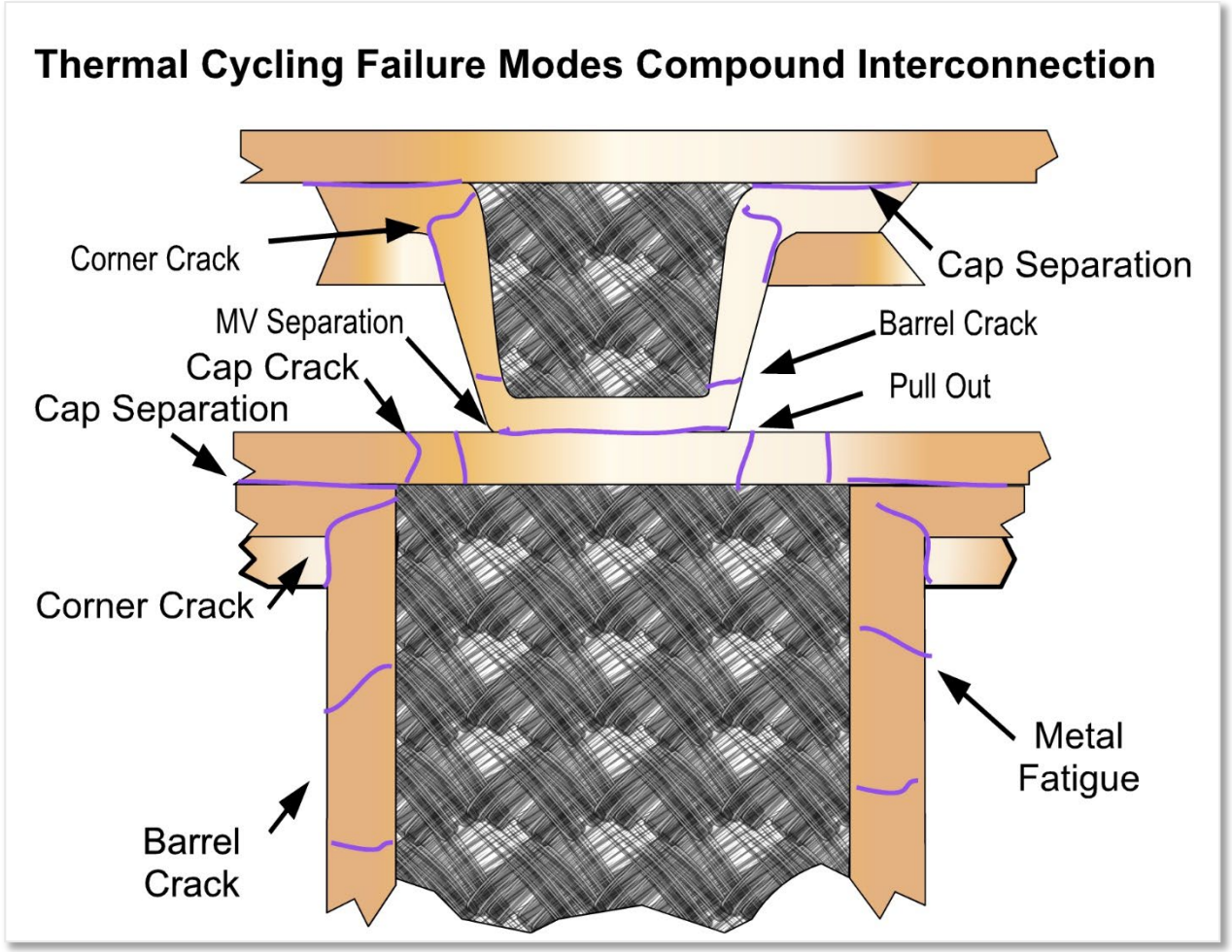




- Damage occurs usually at high temperatures ~ 190°C
- Separation of Capture Pad during contraction

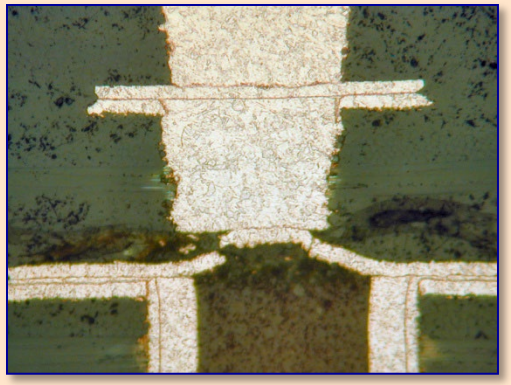
Stacked Microvia - Eight Failure Modes:

- *Separation from Target Pad*
- *Microvia Corner Cracks*
- *Microvia Barrel Cracks*
- *Microvia Pull Out*
- *Cap Crack*
- *Cap Separation (Microvia or Buried Via)*
- *Buried Via Corner Crack*
- *Buried Via Barrel Crack*



Typical Microvia Failure Modes:

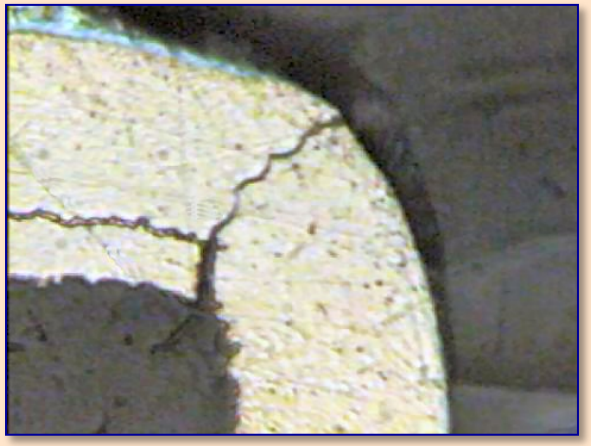
- Target-Pad Separation

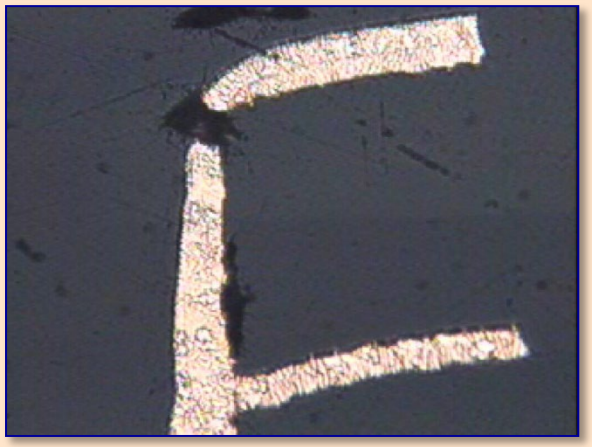


- Capture Pad

- Microvia Corner Cracks

Typical Corner-Cracks:





- Crack in 90° Knee

- more frequent in leadfree technology

- mechanical stress moves to the surface of the PCB.

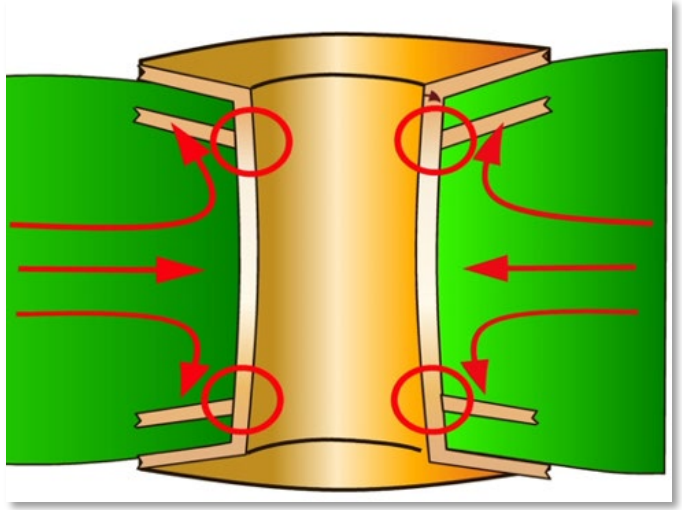
- typically small cracks

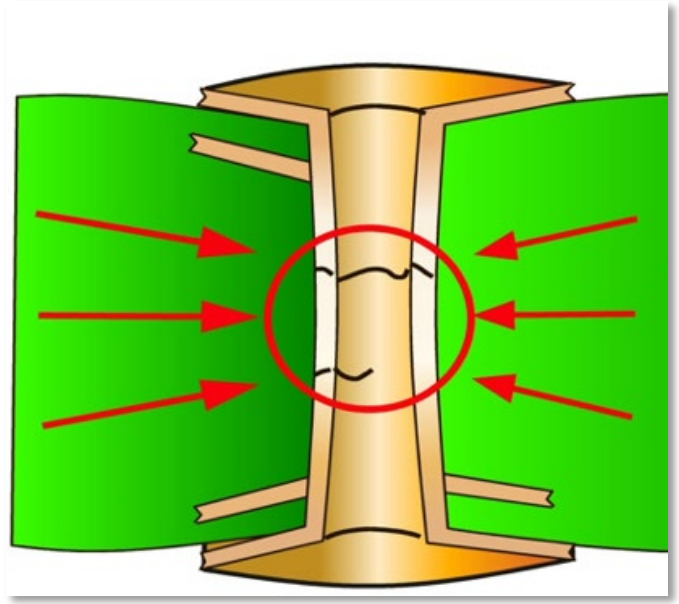
Robustness by Interconnect Type:

1. Microvia are the most robust
2. PTH
3. Blind Vias
4. Buried Vias
5. Complex are the least robust

Robustness by Hole Size:

- Large Holes Stress Interconnect, > .4 mm / .016”
  - Tends to have corner crack or interconnect issues
- Small Holes Stress Barrel, < .4 mm / .016”
  - Tend to have barrel cracks
- Very Small Holes .11 mm / .0045”
  - Tend to be robust, but are prone to crazing



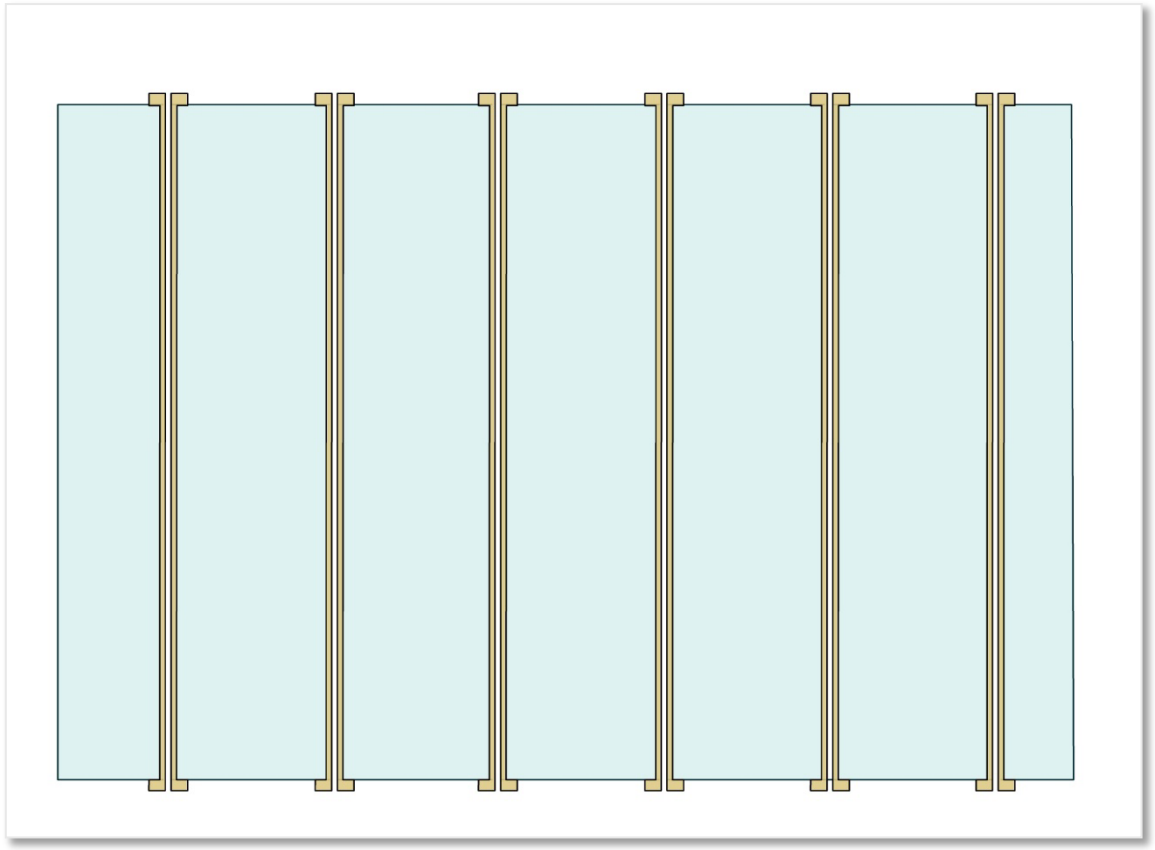


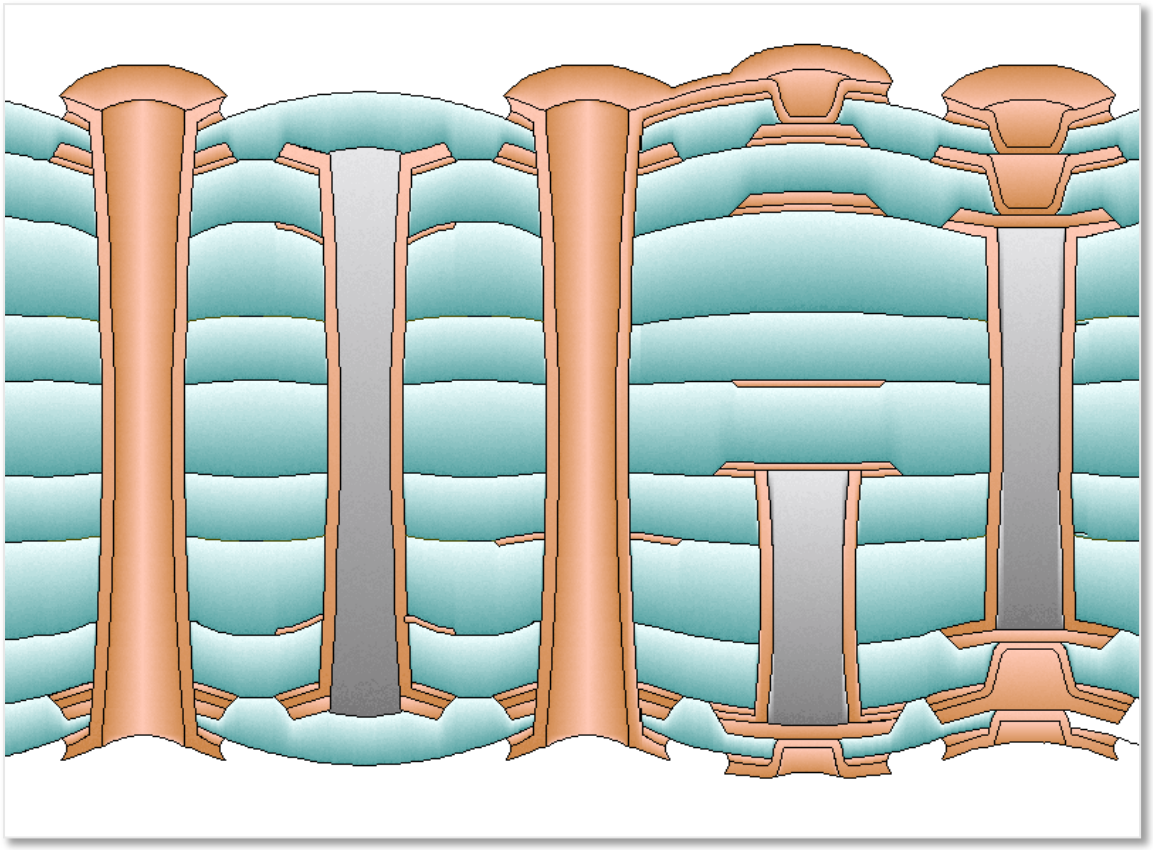
Influence of Grid Size - Material Damage:

- Large Grid 2.5 mm (.100”) - Lower Stress on Material
- Medium Grid 1 mm (.040”) - Adhesive Delamination
- Small Grid .8 mm (.032”) - Cohesive Failure
- Very Small .5 mm (.020”) Grid - Crazing

Influence of a Large Grid Sizes:

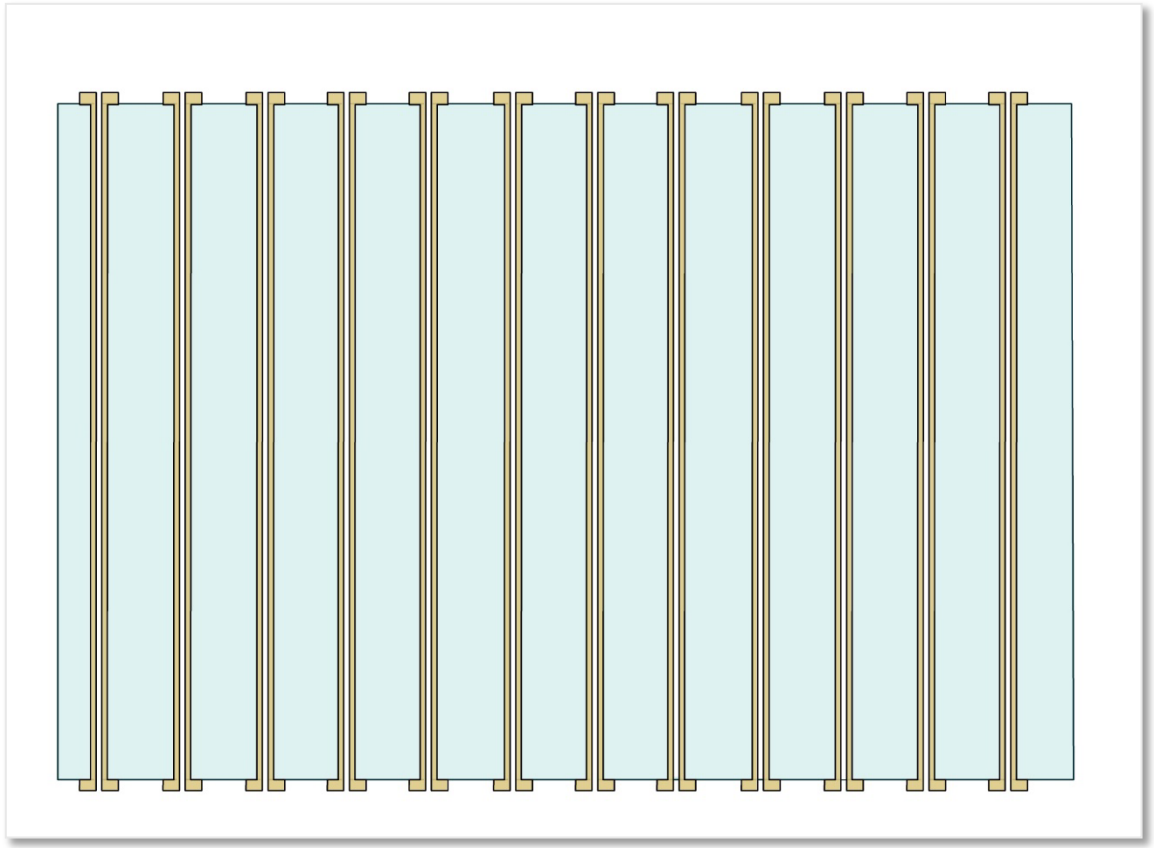
- Large Grid 2.5 mm (.100”) - Stress Relieve Material

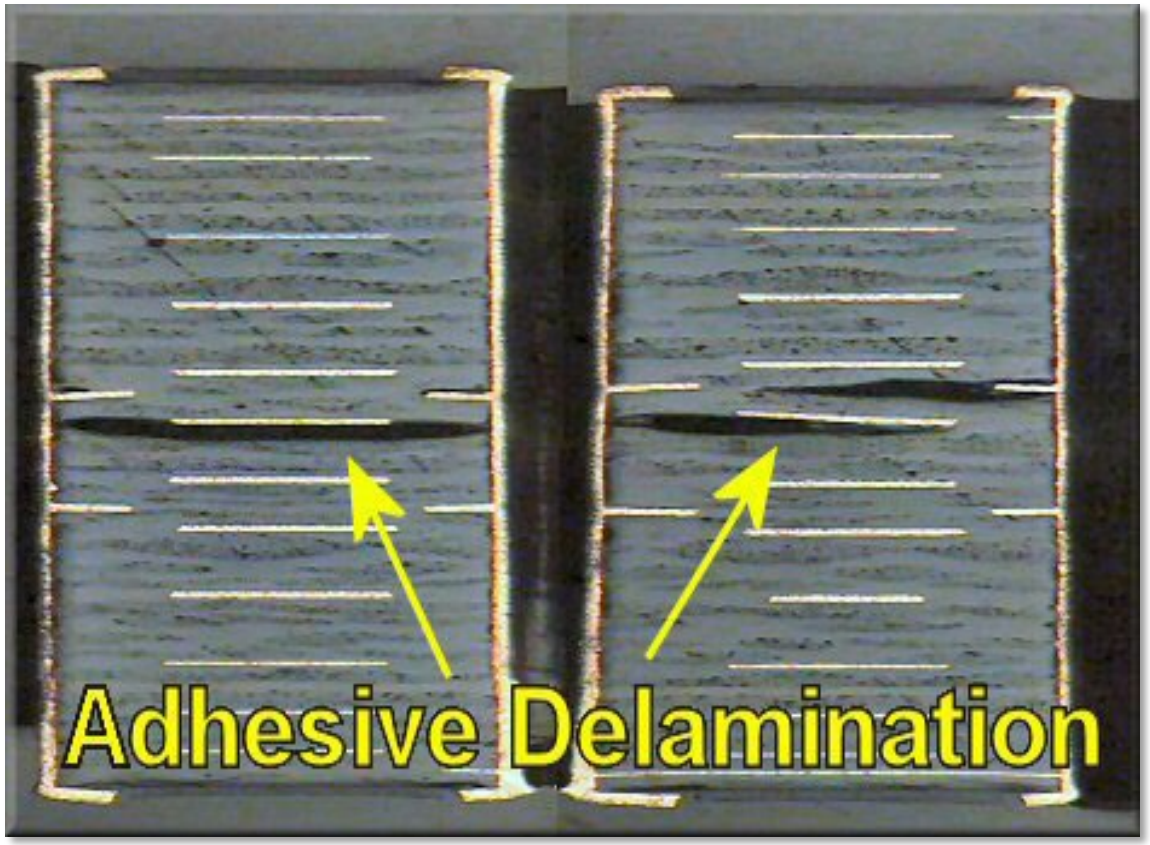




Influence of Medium 1mm / .040” Grid:

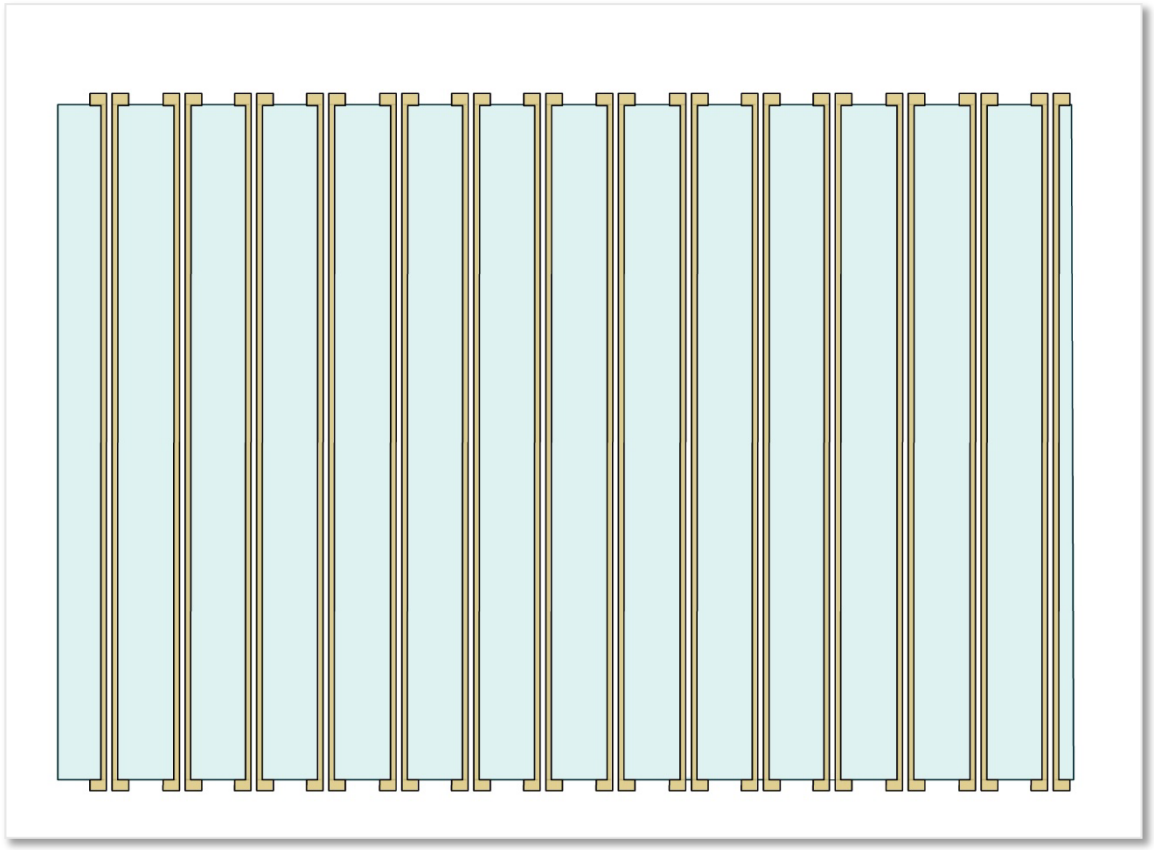
- Medium Grid 1 mm / .040” - Adhesive Delamination

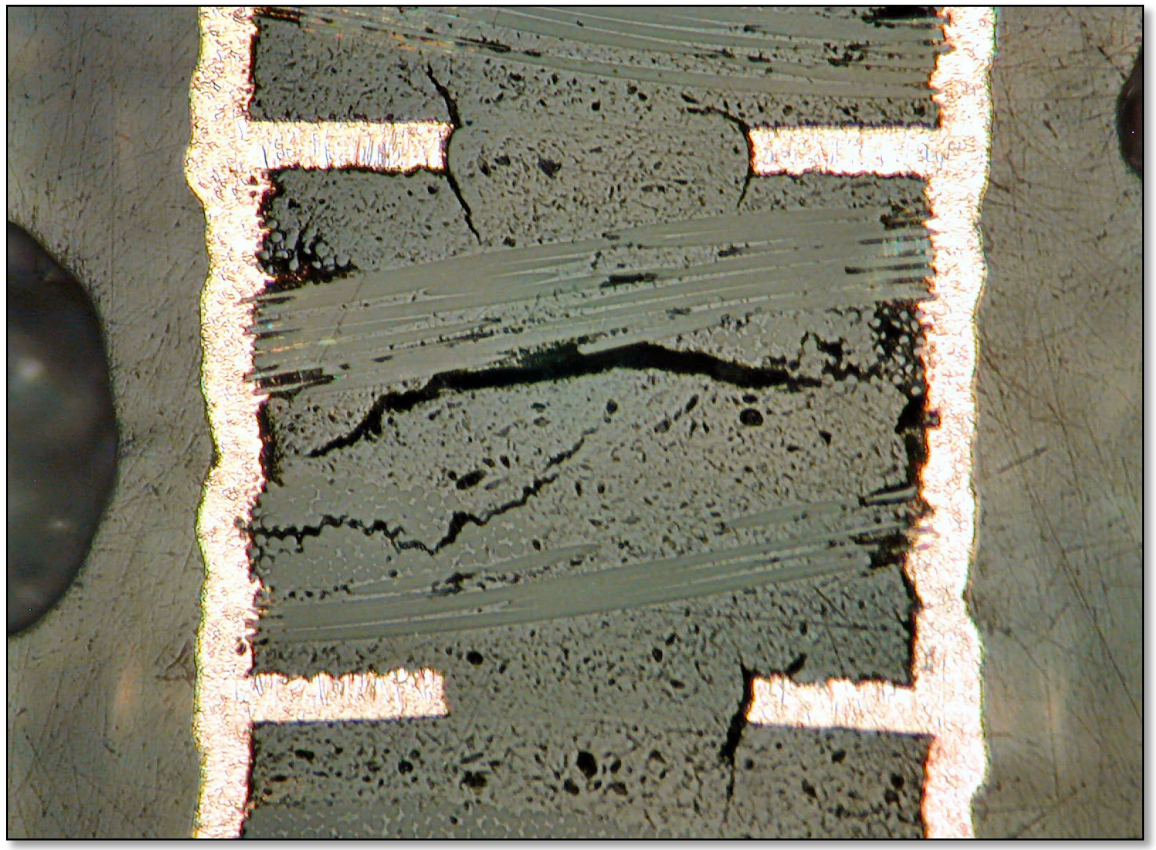




Influence of .032” Grid:

- Small Grid .8 mm / .032” - Cohesive Failure

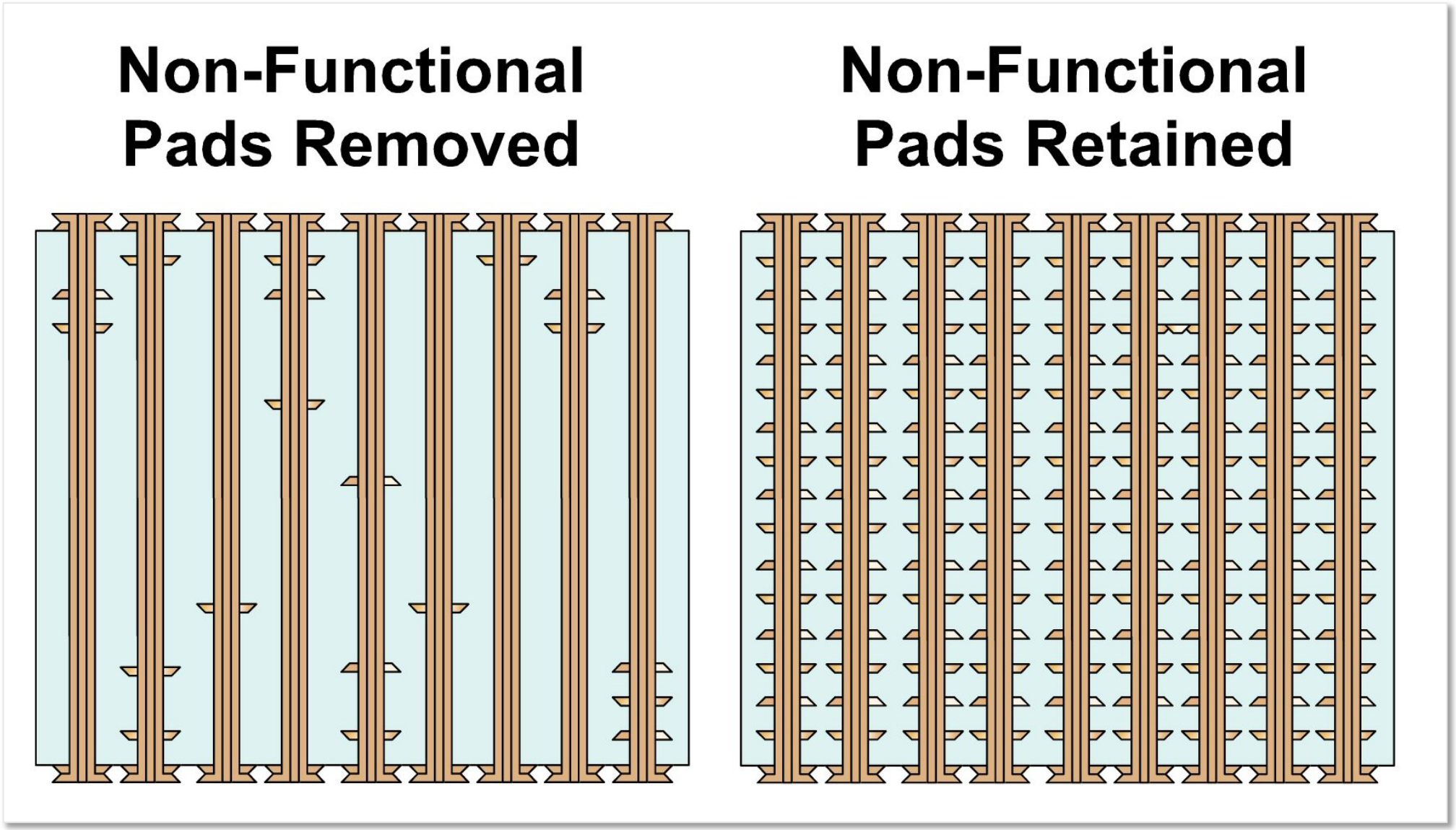




Influence of Non-Functional Pads:

- Non-functional Pad – Have no internal interconnection
- Non-functional Pads In – Reduce Reliability
- Non-functional Pads Out – Increase Reliability
- A few non-functional pads are ok but stay away from the center zone
- Can be used to strengthen back drilling

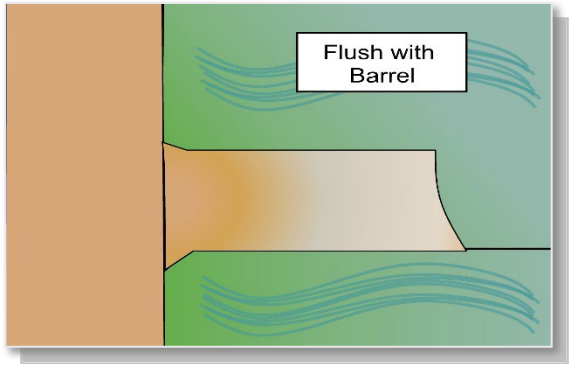
Influence of Non-Functional Pads:

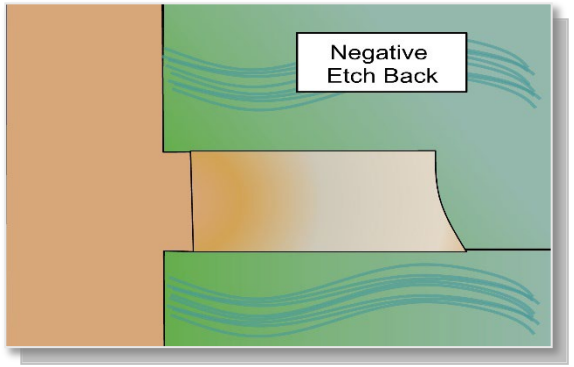


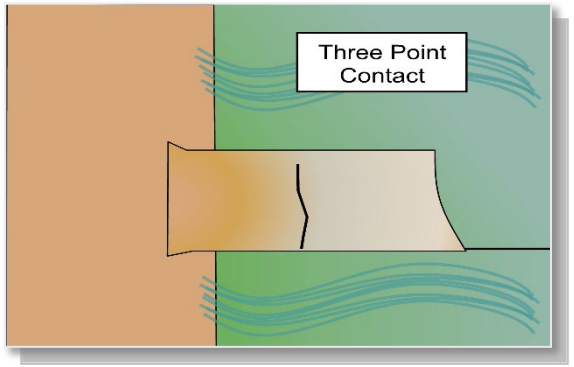
Influence of Type of Interconnections:

Order of robustness:

- Flush with barrel
  - Inner Layer Copper aligns with Dielectric
- Negative Etch Back
  - Inner Layer is Recessed into the Dielectric
- Three point contact
  - Inner Layer Extends into Copper Barrel

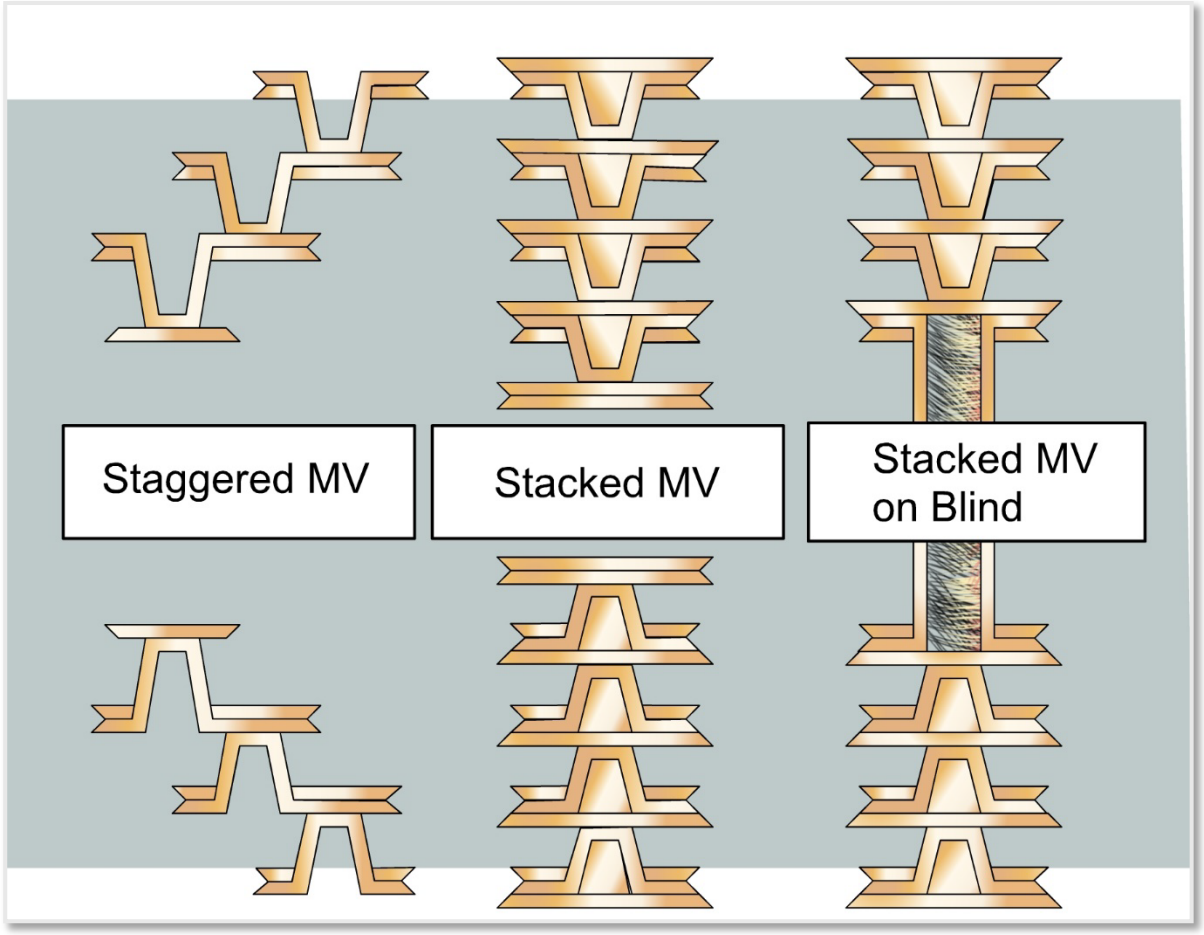






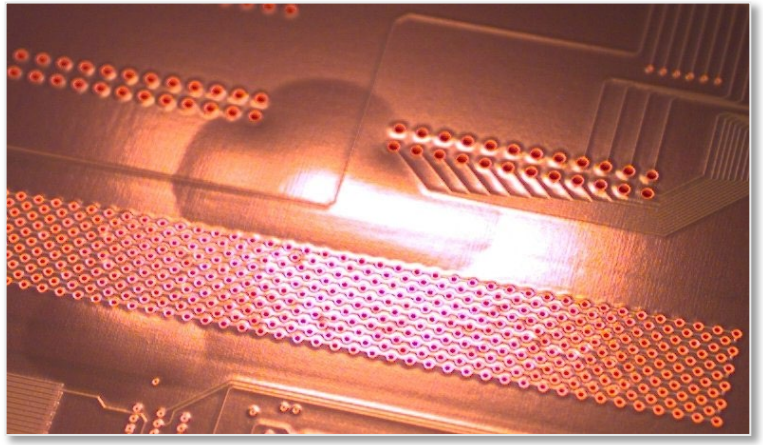
Influence of Microvia Stacked vs. Staggered:

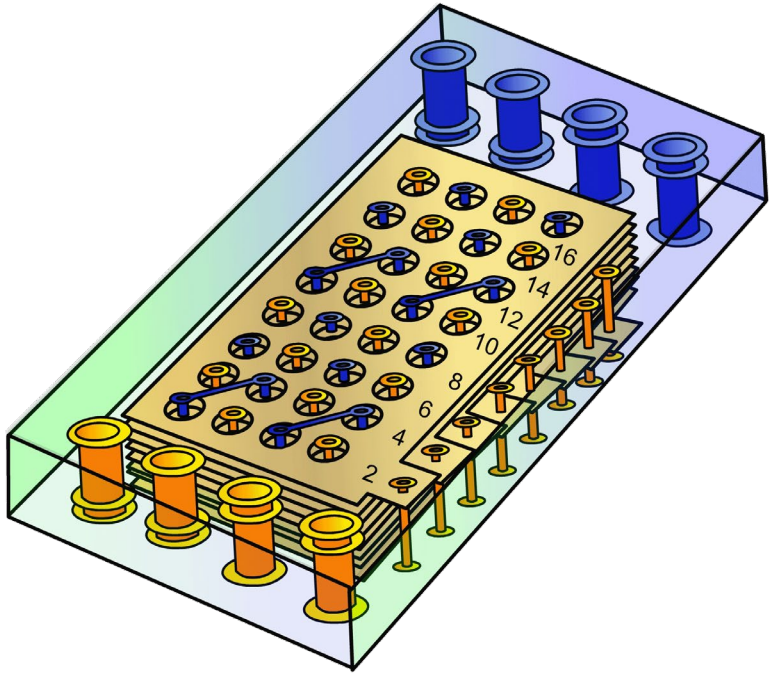
- Three type of compound interconnection
  - Microvia on microvia
  - Microvia on Buried
  - Microvia off Buried
- Staggered Microvias are More Robust
  - The amount of Stagger has no influence
- Stacked Microvias are Less Robust
  - Stack limits differ depending on external variables

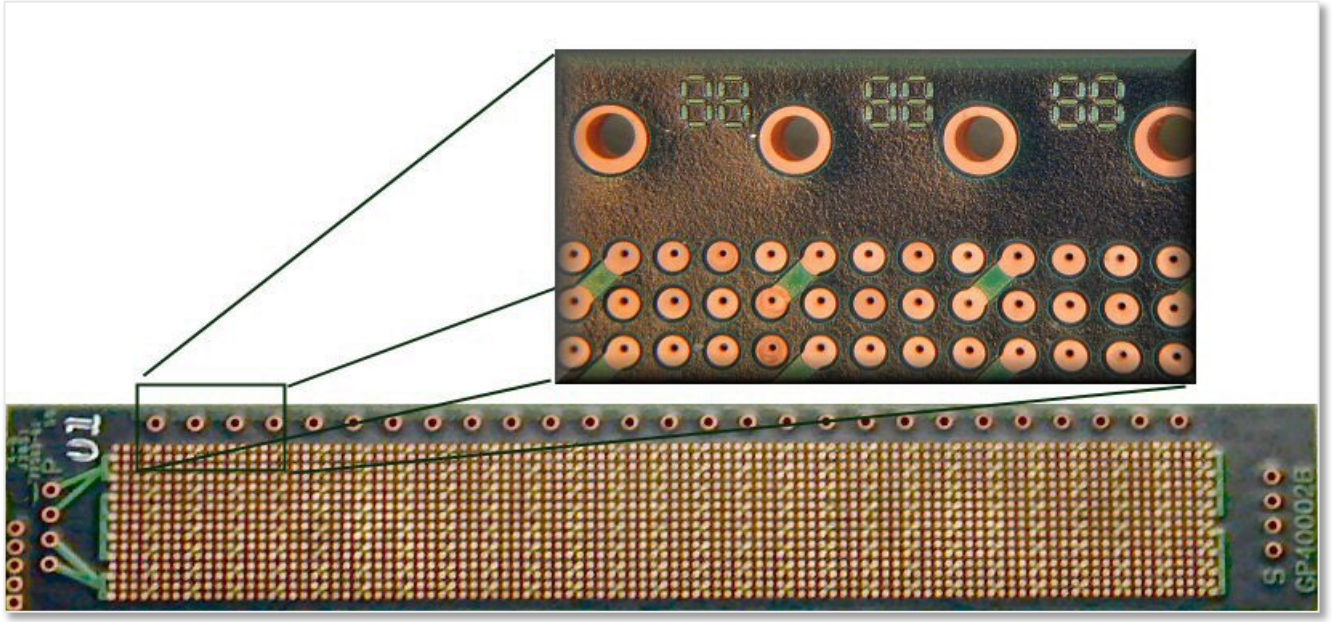


Test for Delamination:

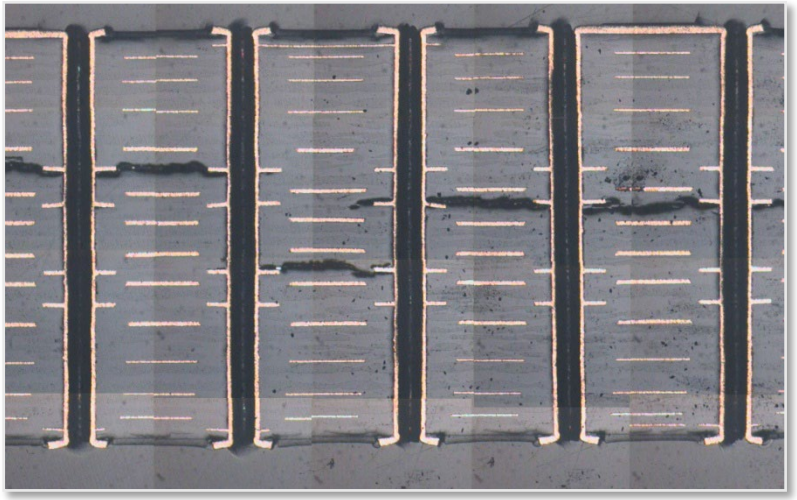
- Checks for Delamination using Capacitance Measurement
- Test Structures integrated in IST Coupon
- Compares Capacitance before and after IST.

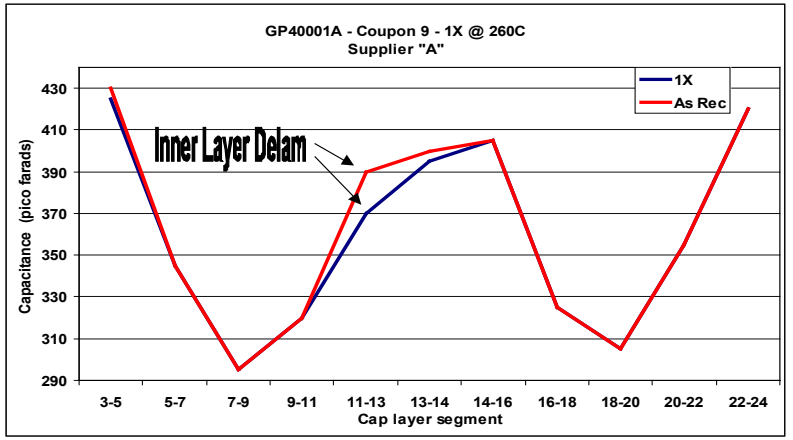




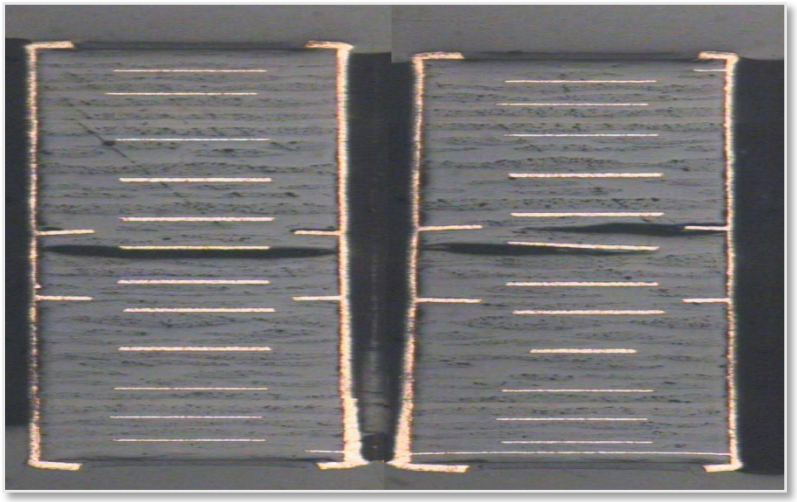


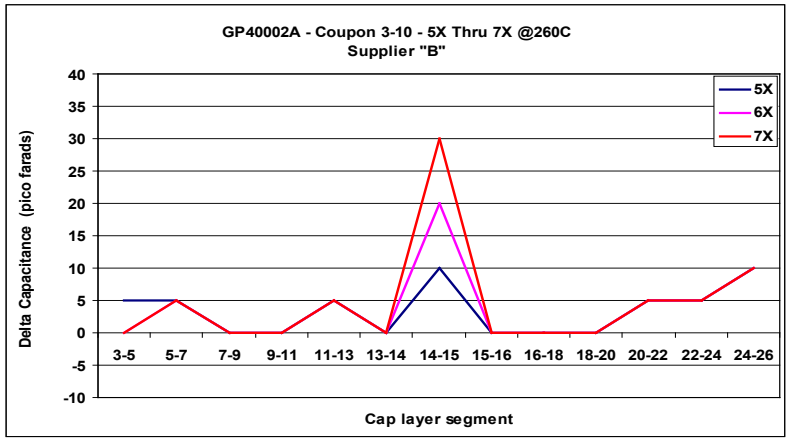
Test for Delamination :





Absolute Capacitance Values before and after IST





Relative change of Capacitance during IST

DELAM-Tester:

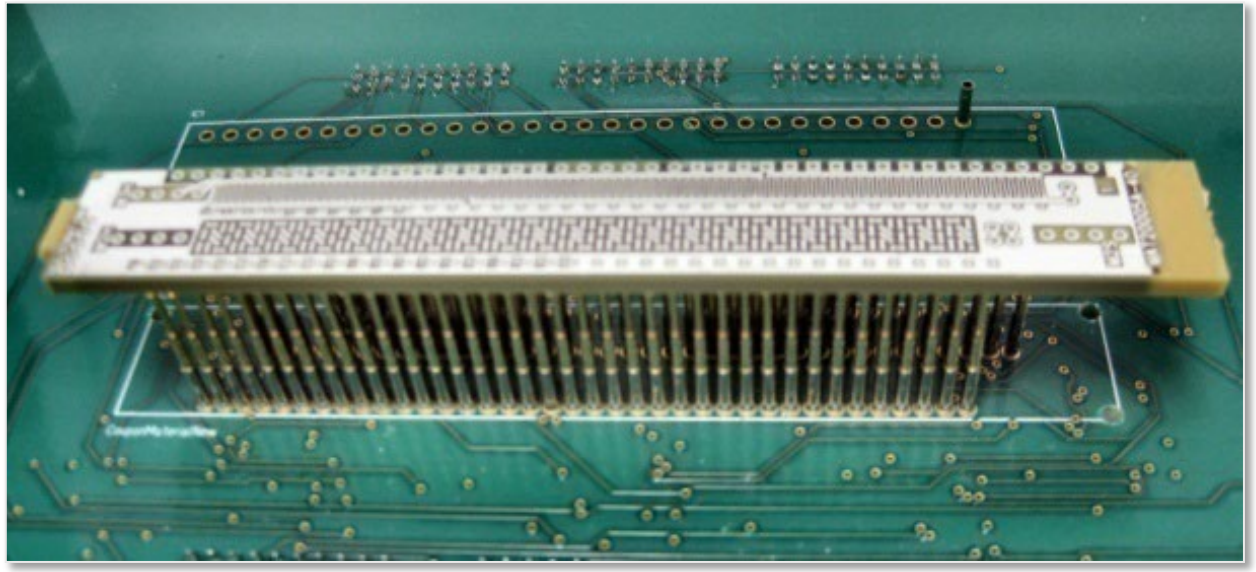
Dielectric

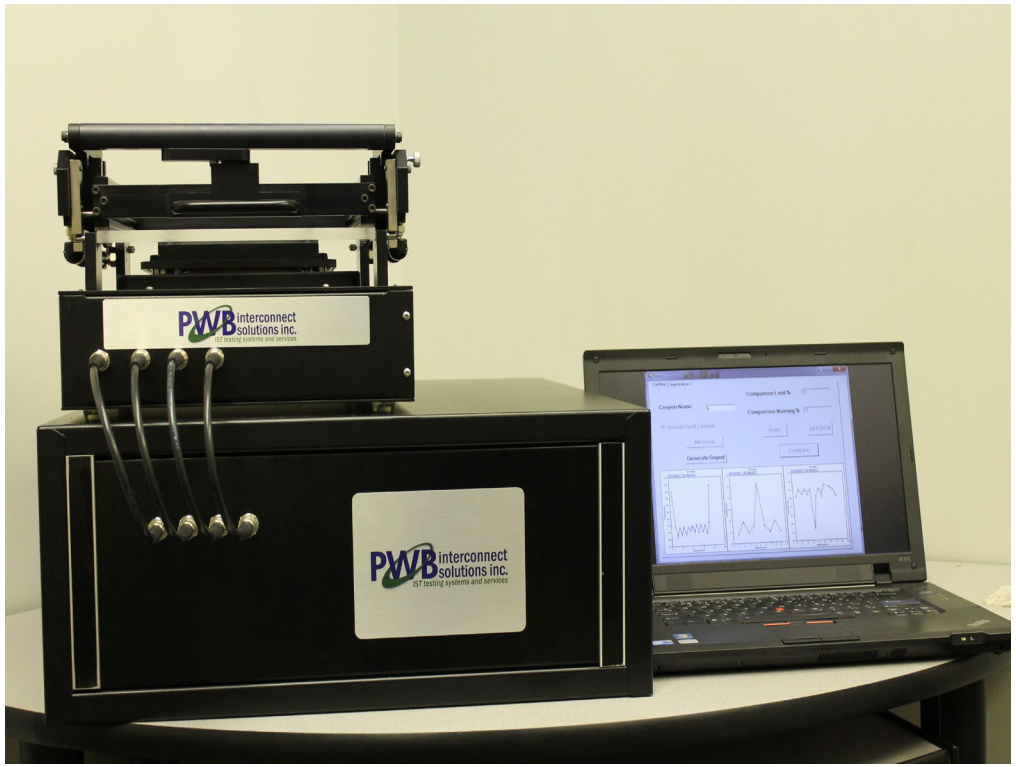
Estimation

Laminate

Assessment

Method

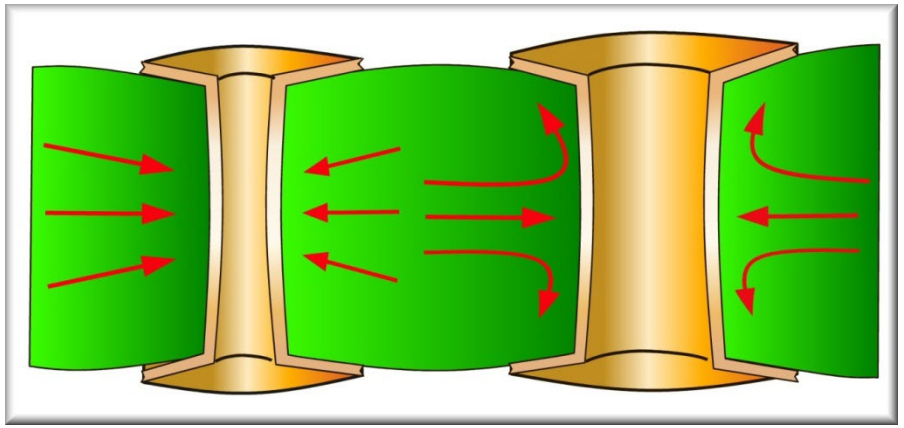




- **PC Controlled**
- **Test Structures integrated in IST Coupon**

Influence Factors on Reliability:

- Temperature
- Via Diameter
- Total PCB Thickness
- Coefficient of thermal expansion (CTE)
- Copper thickness in barrel
- Grid size



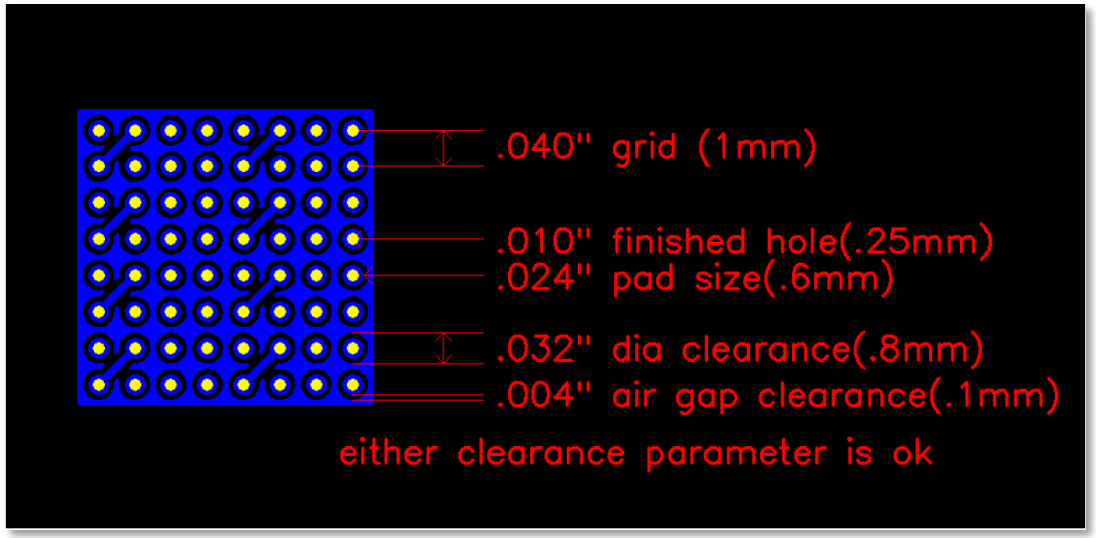
Redistribution of stress depending on via diameter

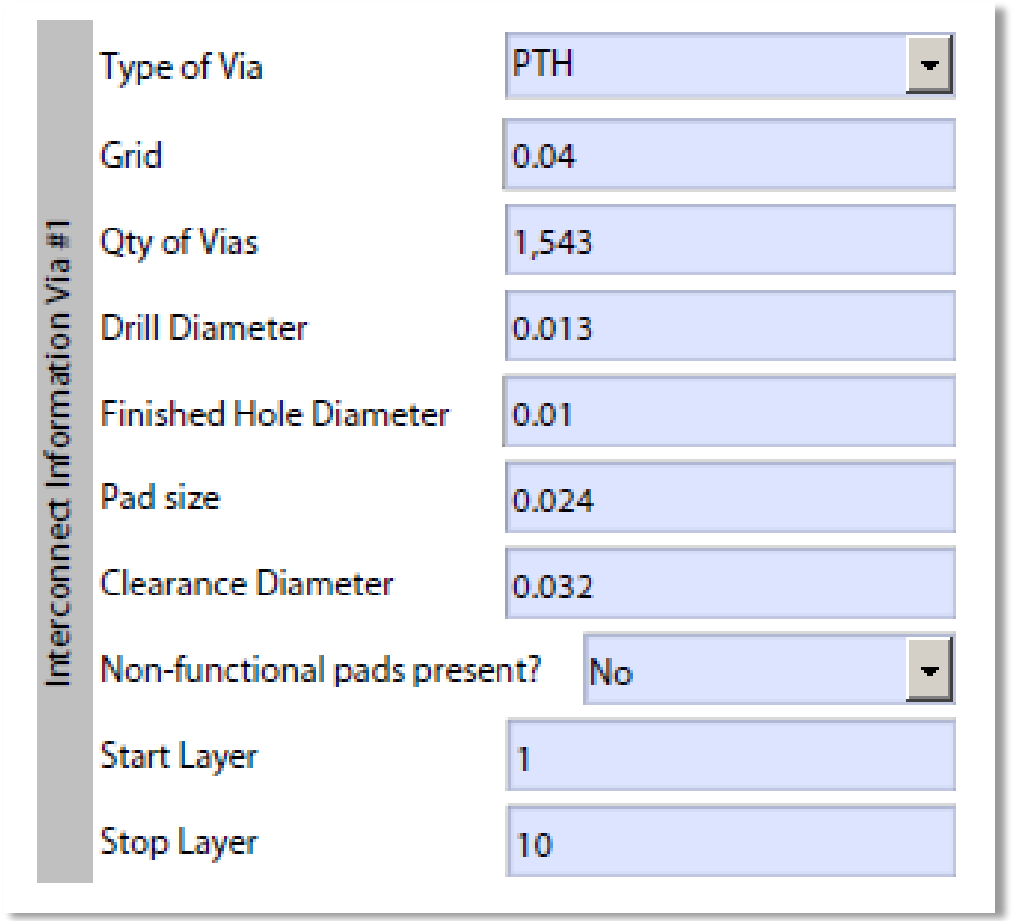
Coupon design is absolutely critical for a representative test

Interconnect Information Via #1

Type of Via (eg. below)	Micro
Grid	.040" (1mm)
Qty of Vias in design	1,482
Drill Diameter	.005" (.127mm)
Finished Hole Diameter	
Pad size	.020" (.5mm)
Clearance Diameter	.030" (.75mm)
Non-functional pads present?	Yes
Start Layer	1
Stop Layer	2

Critical IST Coupon Design Features:





PLATED THRU VIA STRUCTURE FROM CAD INFO
0.010" DIA HOLE THROUGH A .024" DIA PAD
0.032" DIAMETER CLEARANCE IN PLANE
VIAS ON .040" GRID
1543 VIAS OF THIS STRUCTURE IN PWB

Use coupon design worksheet available from
https://polarinstrumentseu.sharepoint.com/:b:/g/Ecyp82wqXCFFunW-JfvFhEkBqRebHoTk9p3kC8pza_ROvg?e=kV3Ppc

IST Interconnect Stress Test is available as a test service and as system installations.

For any questions, please contact:

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