



# Design For Sukses

# Design for suksess

## “Perfekt” design av kretskort

- Finnes perfekte design?
- Hvor må vi gjøre kompromisser?
- Er alle krav og forutsetninger kommunisert og forstått av designteamet? (Tekniske og merkantile suksesskriterier)
- Kan vi kvantifisere konsekvensene av de kompromissene vi tar?
- Tar vi alltid bevisste valg og beslutninger?
- Er CAD verktøyene alltid satt opp korrekt?

| Requirements and Verification plan: JB-1122005 Project X   Doc no:   Author: GG   Rev: 2   Date: 6/10-2022 |                 |                              |  |          |                     |  |                           |                  |
|--|-----------------|------------------------------|--|----------|---------------------|--|---------------------------|------------------|
| Design Requirement Specification   |                 |                              |  |          |                     |  |                           |                  |
| Category   | Requirement id: | Requirement                  | Detailed requirement description   | Priority | Rationale/Reference | Comment  | Verification method       | Stage 1 boundary |
| General  | 1               | Critical Components          | <p>Must use as per Table 2<br/>Components must be installed as per wiring diagram and as per component datasheet.</p> <p>Components with no specific part number may be selected by Kitron, provided they meet the listed specifications in Table 3 and Table 4.</p>   | Must     | Doc-XXXX - Rev Y    |  | Analysis                  |                  |
| General  | 2               | Operating Temperature Rating | <p>Minimum: • Minimum 0°C</p> <p>Maximum:<br/>All components must be within datasheet operating temperatures under the following conditions:</p> <ul style="list-style-type: none"> <li>• 70°C ambient:               <ul style="list-style-type: none"> <li>o no DC current flow</li> <li>o 60% load on AC/DC power supply</li> </ul> </li> <li>• 40°C ambient:               <ul style="list-style-type: none"> <li>o Maximum rated DC current flow</li> <li>o Maximum load on AC/DC power supply</li> </ul> </li> </ul> | Must     | N/A                 | NOTE:<br>A finite nr of components must be selected for temperature logging if customer wants Kitron to do this test. 3rd party involvement will be required | Test performed by Kitron? |                  |

# DFX – Design for X (Excellence)

## Hva er DFX?

En prosess som som ivaretar hensyn til produktets ytelse, driftsmiljø, produserbarhet, testbarhet, kvalitet, logistikkjeder, miljøpåvirkning, regulatoriske krav etc gjennom hele utviklingsløpet.

Sentralt i DFX tankegangen er å forstå hvordan avgjørelser, valg og utførelse påvirker produktet gjennom hele livs syklusen fra konsept til gjenvinning.

En vellykket DFX tilnærming vil muliggjøre effektive tilbakemeldings sløyfer i utvikling og NPI og gi raskere tid til marked og reduserte kostnader gjennom hele levetiden.

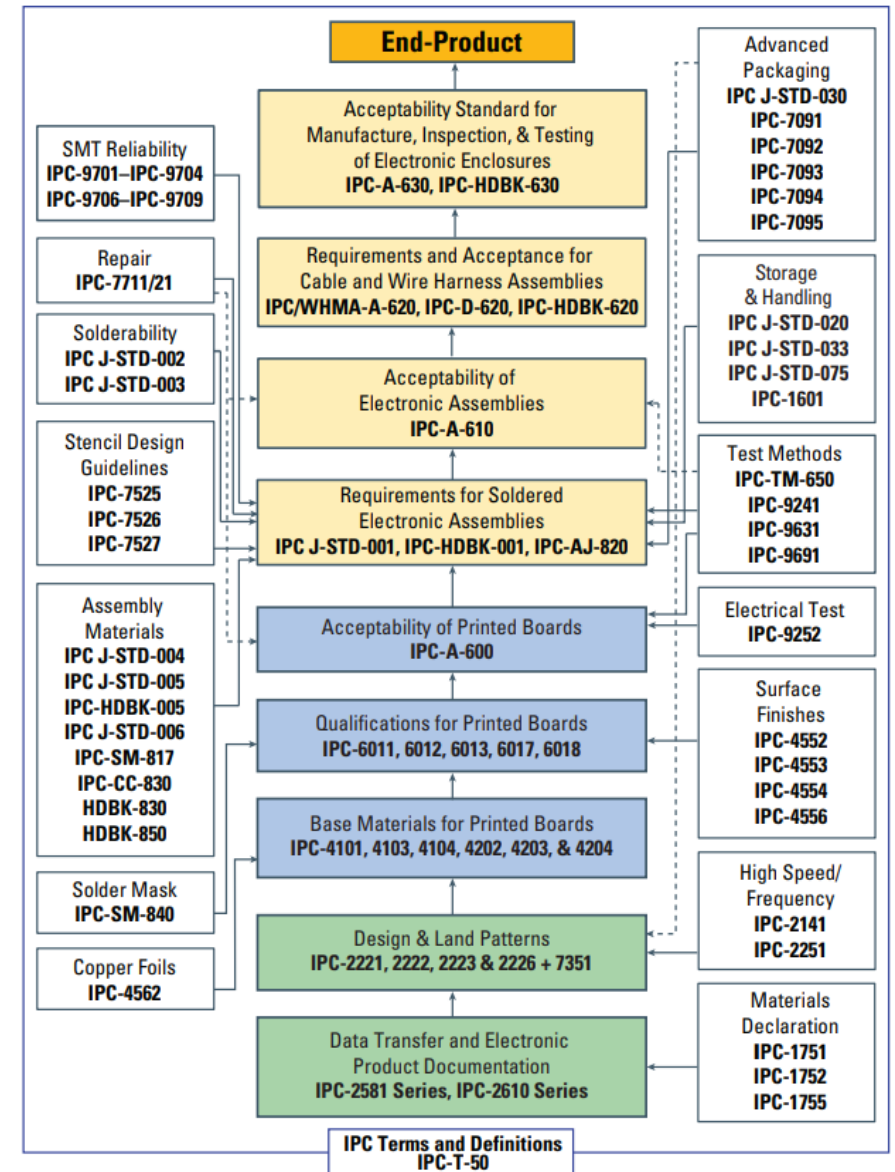
# DFX prosess

Hvordan kommer IPC inn i bildet?

- Utdannelse og sertifiseringer (IPC Edge, IPC PCB design Curriculum, Certified Interconnect Designer)
- Standardisering og retningslinjer (Eg. IPC-2231 DFX guidelines)
- Struktur og sammenheng mellom design, materialer, prosesser og akseptansekrav/kriterier
- Workshops og samarbeid på tvers av industrien

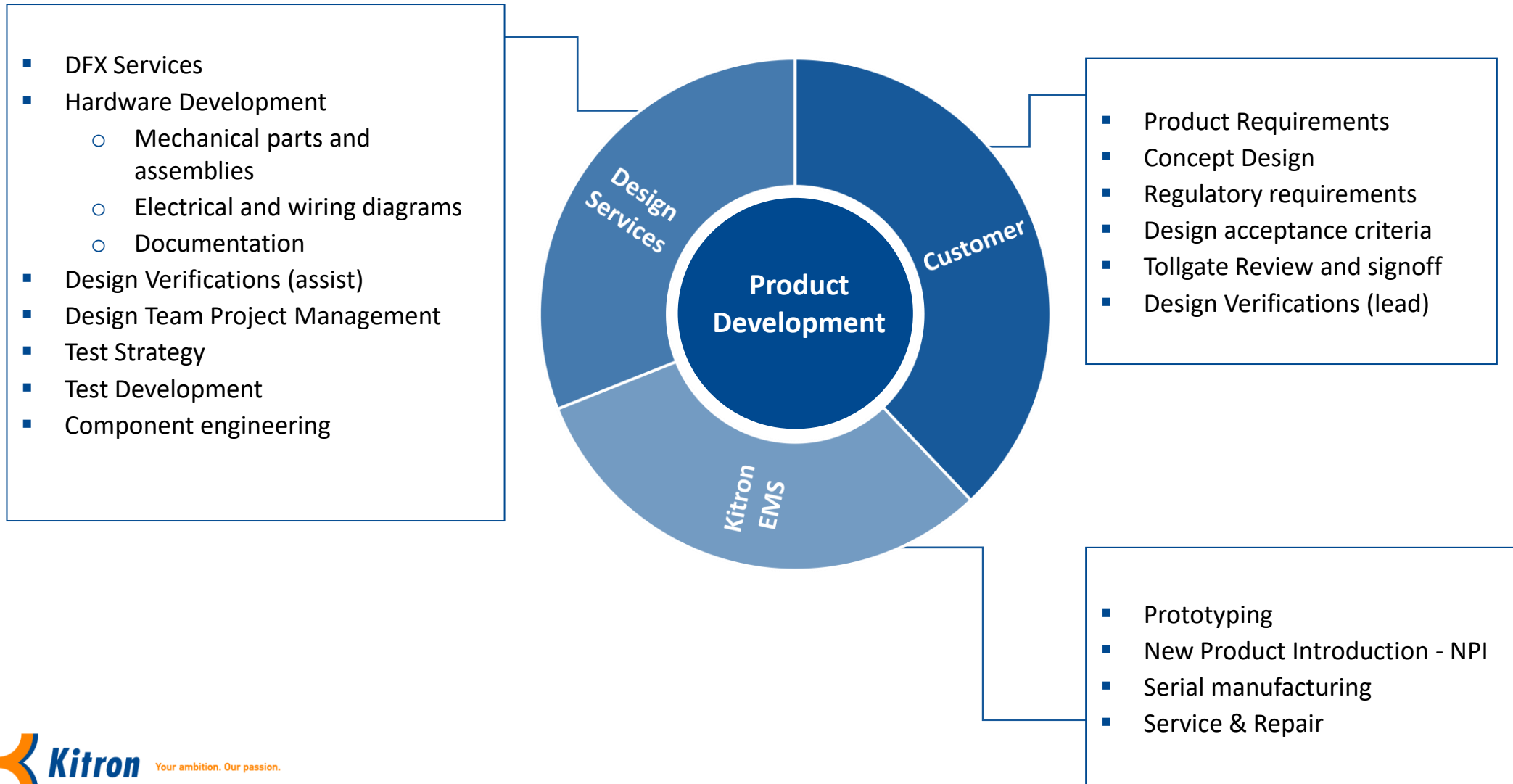


## IPC STANDARDS — EVERYTHING YOU NEED FROM START TO FINISH



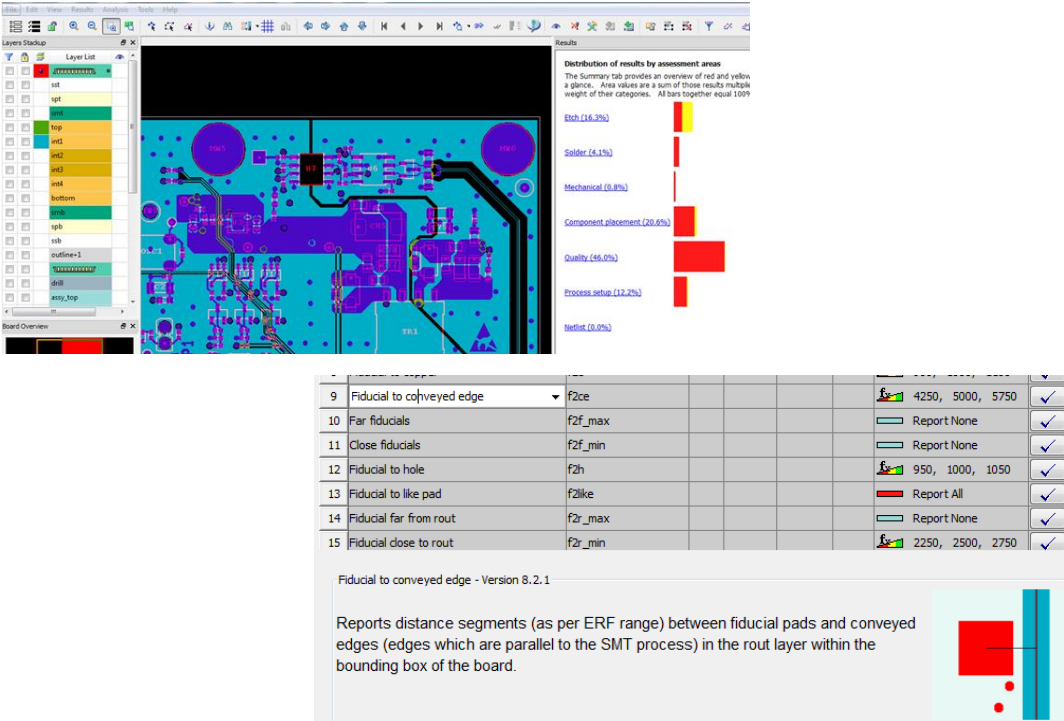
# Kitron's Value Chain Concept

Kitron's value chain combine our technical services portfolio with the manufacturing services, to integrate the design flow with the NPI and manufacturing services



# DFM - Design For Manufacturing Analysis PCBA

- Valor NPI tool analysis for PCB design to optimize Design for Manufacturing
- Identifies potential manufacturing issues before going into production
- Improve manufacturing yields, increase quality
- Reduce the number of design revision spins in the NPI phase
- Cost saving by optimizing board design for cost and manufacturing



|    |                           |         |  |  |  |                  |   |
|----|---------------------------|---------|--|--|--|------------------|---|
| 9  | Fiducial to conveyed edge | f2ce    |  |  |  | 4250, 5000, 5750 | ✓ |
| 10 | Far fiducials             | f2f_max |  |  |  | Report None      | ✓ |
| 11 | Close fiducials           | f2f_min |  |  |  | Report None      | ✓ |
| 12 | Fiducial to hole          | f2h     |  |  |  | 950, 1000, 1050  | ✓ |
| 13 | Fiducial to like pad      | f2like  |  |  |  | Report All       | ✓ |
| 14 | Fiducial far from rout    | f2r_max |  |  |  | Report None      | ✓ |
| 15 | Fiducial close to rout    | f2r_min |  |  |  | 2250, 2500, 2750 | ✓ |

Fiducial to conveyed edge - Version 8.2.1

Reports distance segments (as per ERF range) between fiducial pads and conveyed edges (edges which are parallel to the SMT process) in the rout layer within the bounding box of the board.

| Valor NPI tool assessments | Additional DFM assessments       |
|----------------------------|----------------------------------|
| - Fiducial analysis        | - PCB specification              |
| - Component analysis       | - Layer stackup check            |
| - Padstack analysis        | - THT solderability              |
| - Test point analysis      | - PCB complexity assessment      |
| - Solderpaste analysis     | - Teardrop check                 |
| - Netlist analysis         | - Selective soldering assessment |

*Input needed: PCB files with preferred file format ODB++ or IPC-2581*

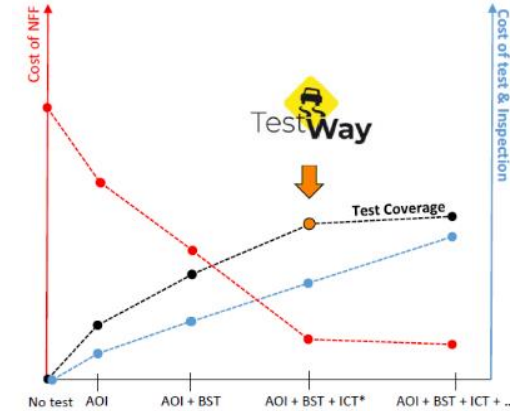
*(Note: Gerber file format will not contain all info needed for complete analysis)*

# DFT - Design For Testability Analysis PCBA

- Testability analysis for PCBA using TestWay:
  - Test coverage estimations for different combinations of tests and inspections to improve product design for testability
  - Design for Test recommendations
- Required input:
  - Intelligent CAD data (ODB++, GenCAD, IPC-2581 or similar)
  - Schematics and BOM

## TestWay – Test Coverage Analyzer & Simulator

Test Strategy Simulation  
Design for Testability  
Predictive Test Coverage  
Test Report Automation



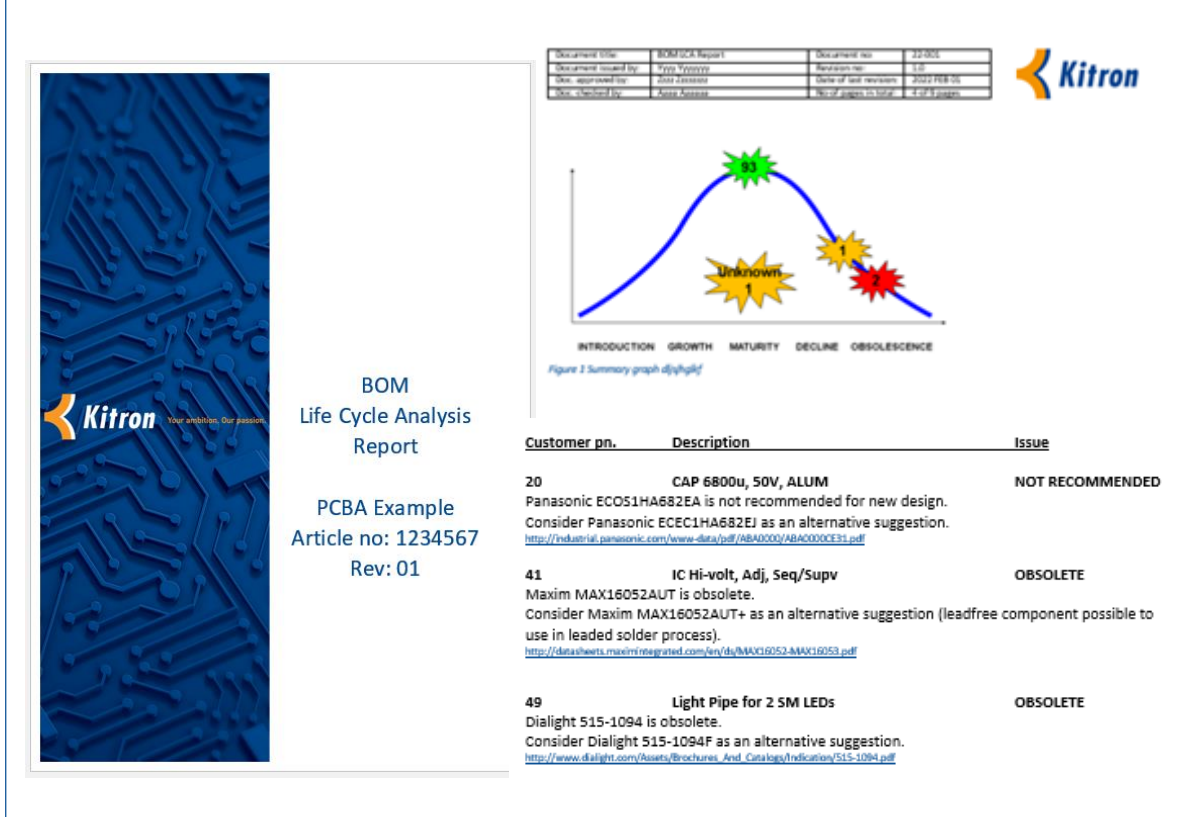
The screenshot shows the 'Test line editor' window. It is divided into three main sections:

- Coverage estimation for theoretical tester:** A grid of icons representing different test methods. 'BST' is highlighted with a blue bar.
- Real coverage from test program:** A grid of icons representing test equipment. 'FCT' is highlighted with a blue bar. Other equipment like 'a3Di', 'acculogic', 'asset', 'bfx2', and 'bsi' have red 'X' marks, indicating they are not supported or not used.
- Test line:** A sequence of test steps: 'AOI' → 'FPT' → 'BST'. Each step has a green checkmark below it, indicating successful completion.

On the right side, there are buttons for 'Analyze', 'View report', 'Close', and 'Help', along with a 'Classifier' gauge.

# BOM analysis - Life Cycle Health

- Kitron's Life Cycle Analysis (LCA) is a structured process to assess electronics components in BOM
- Life Cycle Analysis includes:
  - Components Life Cycle status (Active, Obsolete, LTB Date, NRND)
  - Single source identification
  - Second source suggestions
- BOM Life Cycle Management programs (For Kitron AS production programs):
  - Continuous monitoring of risk components
  - Early warnings enable obsolete planning
  - Define last-time buy strategies
  - Input and support for Re-design and verifications of component changes



**BOM Life Cycle Analysis Report**

PCBA Example  
Article no: 1234567  
Rev: 01

| Document title     | BOM LCA Report | Document no.          | 22-001       |
|--------------------|----------------|-----------------------|--------------|
| Document issued by | Yves Yoccoz    | Revision no.          | 1.0          |
| Doc. approved by   | Alex Assouad   | Date of last revision | 2022 FEB 05  |
| Doc. checked by    | Alex Assouad   | No. of pages in total | 4 of 3 pages |




Figure 1 Summary graph d3y4gk4f

| Customer pn. | Description   | Issue           |
|--------------|---|-----------------|
| 20           | CAP 6800u, 50V, ALUM<br>Panasonic ECOS1HA682EA is not recommended for new design.<br>Consider Panasonic ECEC1HA682EJ as an alternative suggestion.<br><a href="http://industrial.panasonic.com/www-data/pdf/ABA0000/ABA0000CE31.pdf">http://industrial.panasonic.com/www-data/pdf/ABA0000/ABA0000CE31.pdf</a>                               | NOT RECOMMENDED |
| 41           | IC Hi-volt, Adj, Seq/Supv<br>Maxim MAX16052AUT is obsolete.<br>Consider Maxim MAX16052AUT+ as an alternative suggestion (leadfree component possible to use in leaded solder process).<br><a href="http://datasheets.maximintegrated.com/en/ds/MAX16052-MAX16053.pdf">http://datasheets.maximintegrated.com/en/ds/MAX16052-MAX16053.pdf</a> | OBSOLETE        |
| 49           | Light Pipe for 2 SM LEDs<br>Dialight 515-1094 is obsolete.<br>Consider Dialight 515-1094F as an alternative suggestion.<br><a href="http://www.dialight.com/Assets/Brochures_And_Catalogs/indications/515-1094.pdf">http://www.dialight.com/Assets/Brochures_And_Catalogs/indications/515-1094.pdf</a>                                      | OBSOLETE        |



# Suksessfaktorer

## Automatisering

- Mest mulig maskinmonterbare komponenter f.eks SMT, PiP
- Tilstrekkelig frirområde for selektiv lodding der en må bruke hullmonterte komponenter
- Designe for robotlakkering der det er mulig
- Utviklet test strategi, også med hensyn på programmering
- Enkel håndtering av mekaniske komponenter (High Level Assembly)



- Examples of desirable design features:
  - Design for robot gripper handling
  - Minimize use of non-rigid components
  - Vision system positioning and orientation
  - Top-down, z-axis, assembly is often a preferred design solution

# Suksessfaktorer

## Produksjonsprosesser

- Unngå bruk av «ekstra prosesser», for eksempel fjerning av elektrolytisk gull fra komponenter
- Velg komponenter som tåler prosessene, f.eks tetthetsklasse, temperatur, antall loddecycler etc
- Velg hensiktsmessige komponenter, f. eks konnektorer som er tette i bunn ved lakkering av kretskort (conformal coating)
- Reduser antall prosesstrinn mest mulig, f eks SMD kun på en side
- Sett opp designregler og komponentbibliotek i CAD fornuftig i forhold som har betydning for montasje og loddeprosesser

### Recommended PCB Reliability Guidelines



package substrate. These **vent** holes are kept by design between the heat spreader (lid) and the package substrate to allow for outgassing and moisture evaporation.

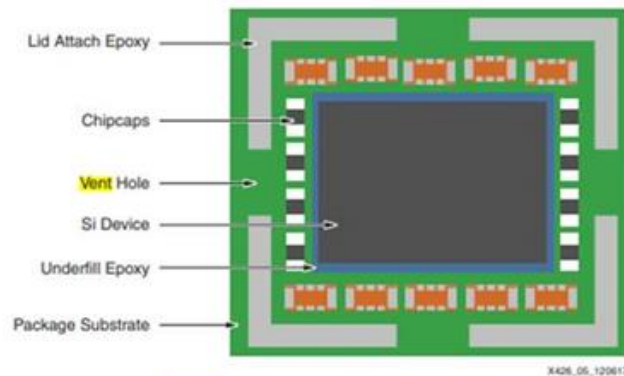
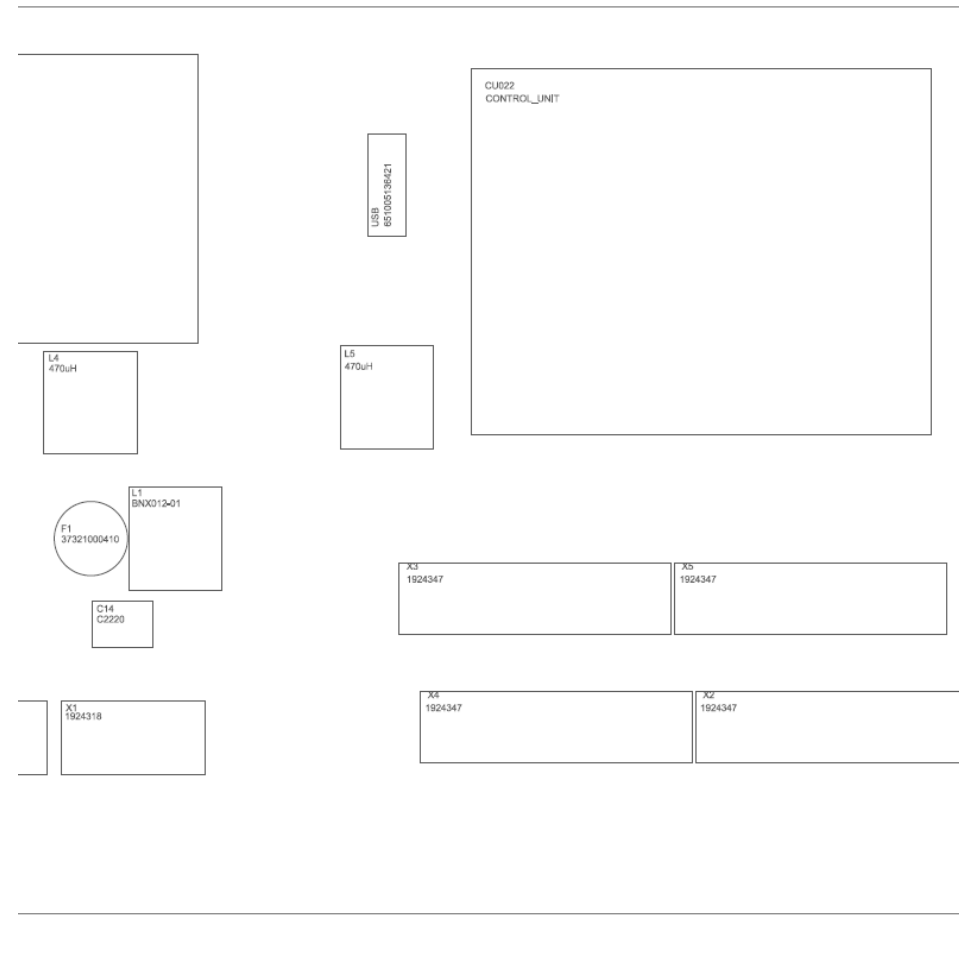


Figure 5: Example of **Vent** Holes and Chip Capacitors (Package Dependent)

# Suksessfaktorer

## Dokumentasjon

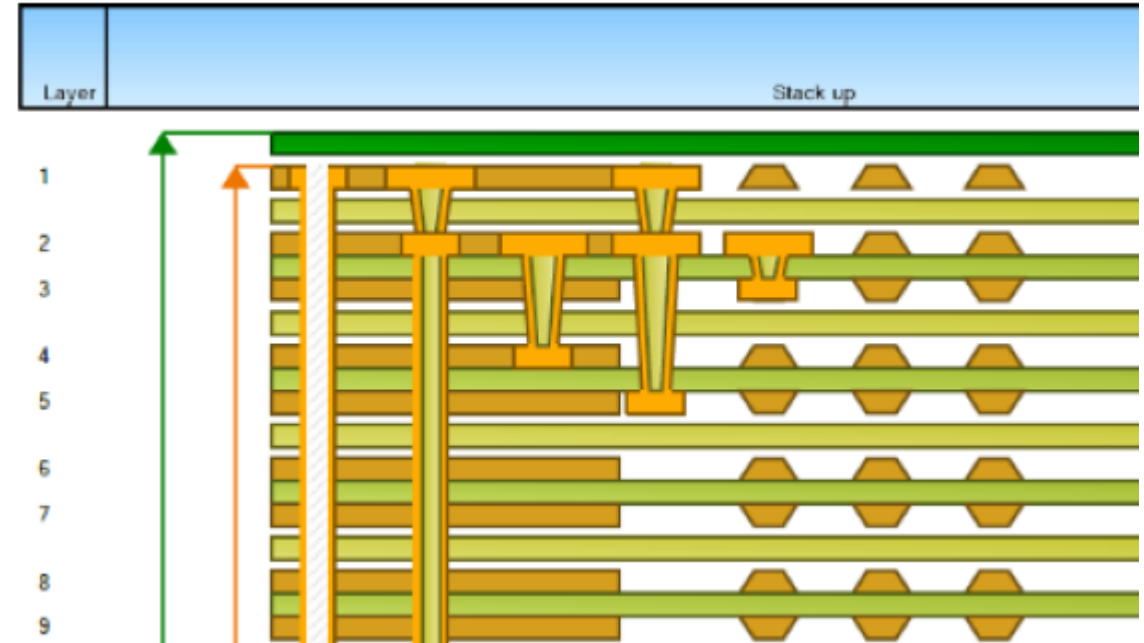
- Identifiser alle spesielle forhold og dokumentér med noter på tegning, f.eks komponenter som ikke tåler vask, har temperaturklassifisering under grenseverdier i J-STD-020, liming, utførelseskrav, tiltrekkingsmomenter etc
- Inkluder generiske CAD filer (ODB++, IPC-2581) når det er mulig
- Komponentplasseringstegning må være tydelig, f eks pinne 1 markering vs katode for LEDer kan føre til feiltolkning av polaritet
- Ha alternativer for alle komponenter der det er mulig, eventuelt spesifiser generisk i BOM
- Dokumentér separate prosesser der det er hensiktsmessig, f eks ikke kombinér komponentplasseringstegning og maskeringstegning om denne inneholder mye informasjon
- Lever søkbare filer, f eks vektorisert PDF
- 3D modeller, f eks 3D pdf kan være nyttig ved komplekse sammenstillinger
- Ha tilstrekkelig konfig styring og dokumentér endringer



# Suksessfaktorer

## Kompleksitet og design features

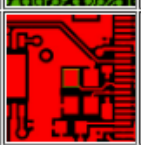

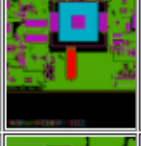
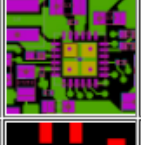


- Unngå suboptimalisering
- Unngå overspesifisering
- Ikke utfordre for mange kapabiliteter i samme design
- Verifiser løsninger som ikke er standard med leverandørene
- Ikke begrens tilgjengeligheten av leverandører unødig
- Unngå unødig blanding av teknologier, f eks veldig små komponenter på power kort eller før nær store eller komponenter som krever mye loddepasta



# Eksempler fra DFM og NPI

## Gradering av alvorlighet (Produksjonsteknisk perspektiv)

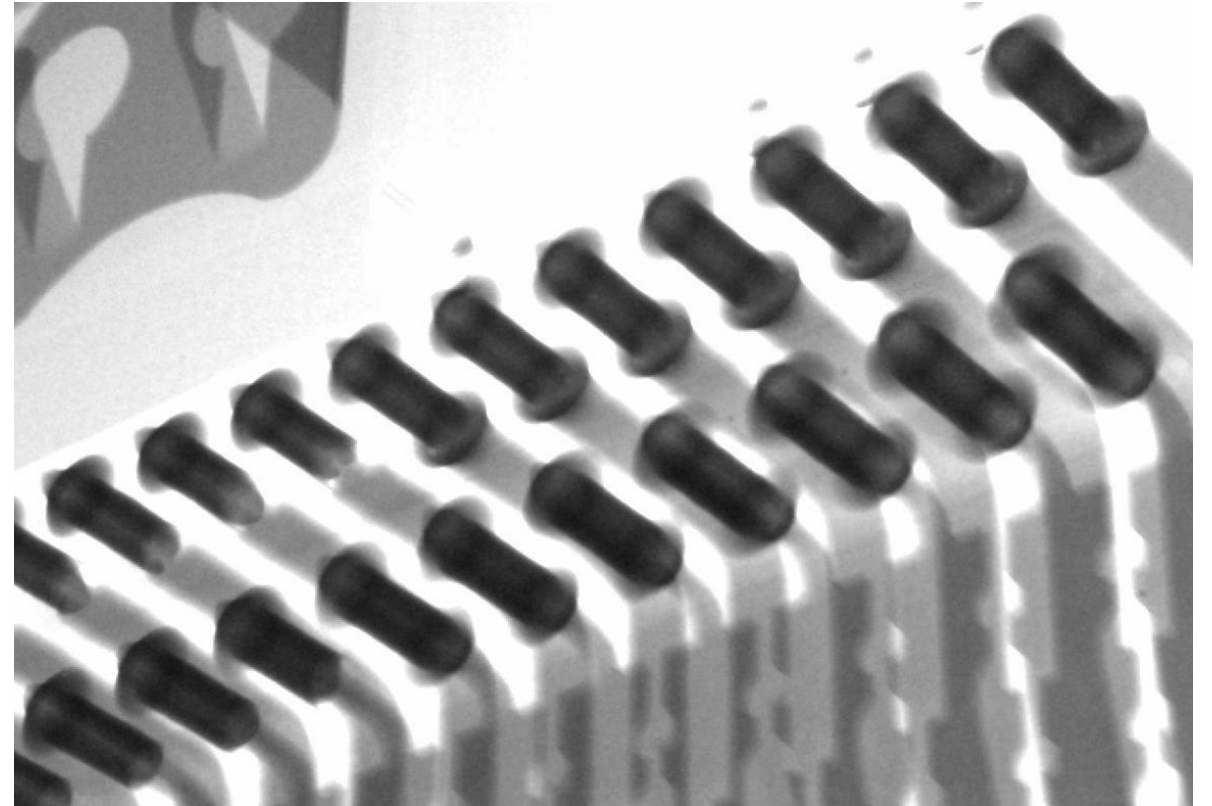
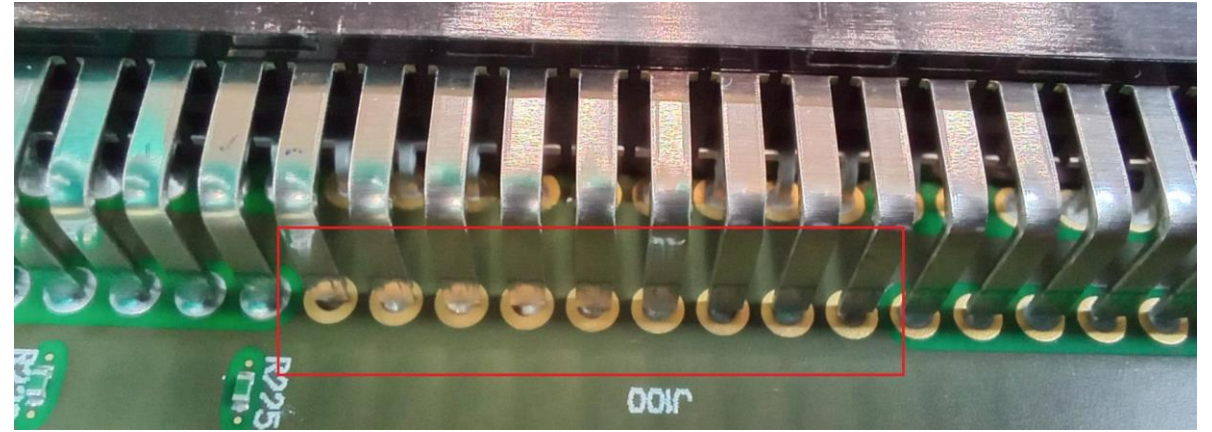
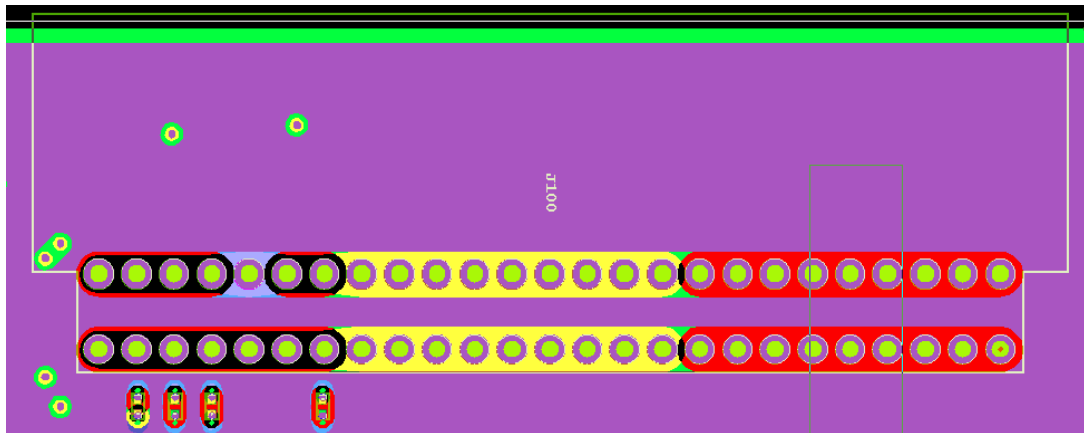
- Critical: The product is not manufacturable as it is, reported issues must be verified and amended before ordering PCBs or starting production.
- Hot: High risk. Will likely cause poor yield, higher cost, quality risks and non-compliance to workmanship standards.
- Warm: Medium risk. Should be observed and evaluated during preproduction and evaluated on prototype run to verify whether a design change is recommended
- Cool: Low risk, for information.
- Ignore: For information only.

|    |                                     |        |  |        |          |           |  |   |
|----|-------------------------------------|--------|--|--------|----------|-----------|--|---|
| 5  | chk:Nets without testpoints         | opened |  |        | cool     | 1.150010  |   | 2 |
| 6  | chk:Testpoint to toeprint R93       | opened |  |        | hot      | 0.405240  |   | 1 |
| 7  | Testpoints on both sides            | opened |  |        | cool     |           |  |   |
| 8  | chk:SP not exposed by soldermask    | opened |  |        | critical | 3.424762  |   | 4 |
| 9  | chk:SP not exposed by soldermask    | opened |  |        | critical | 1.074600  |   | 5 |
| 10 | chk:Roof Area / Wall Area (feature) | opened |  |        | warm     | 11.682000 |   | 5 |
| 11 | chk:Roof Area / Wall Area (feature) | opened |  | Kitron | warm     | 12.612000 |  | 7 |

# Eksempler fra DFM og NPI

## Loddbarhet hullmonterte komponenter

- Manglende thermal relief
- For stor web bredde (IPC-2222 9.0)
- For stor kumulativ web bredde
- For liten hulldiameter/capillary gap (IPC-2222 Table 9-3)
- Bør en akseptere mindre enn 100% solder fill på prototype?

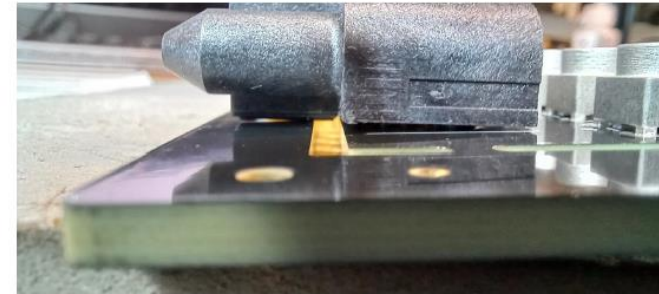
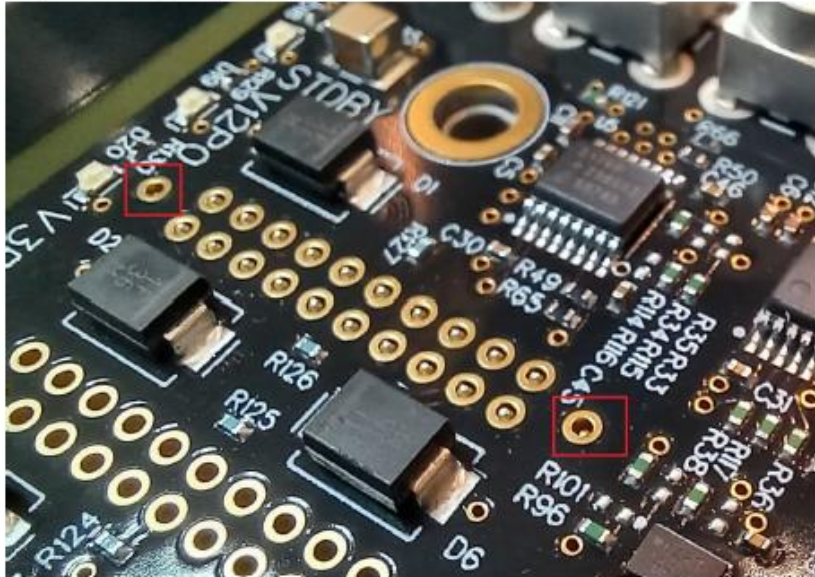


# Eksempler fra DFM og NPI

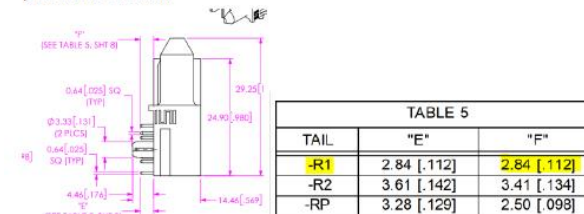
## Feil pinnelengde på hullmonterte komponenter

- Sjekk mot datablad
- Velg den varianten som er nærmest men lite utstikk er bedre enn for mye ved selektiv lodding

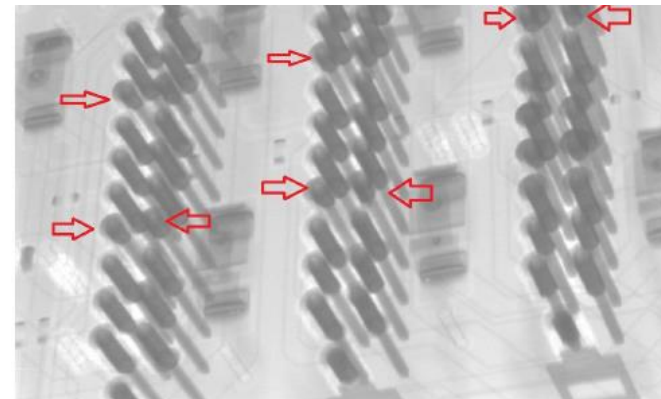
There are no leg protrusions on guide pins on pos J14 to J17, SH100005479 and SH100005676 and vary little on regular pins, approx. 0,08mm.



There are no leg protrusions on pins on pos J1, SH100005530, ET60T-D08-5-02-000-S-R1-S. R1 has pins that are 2,84mm.



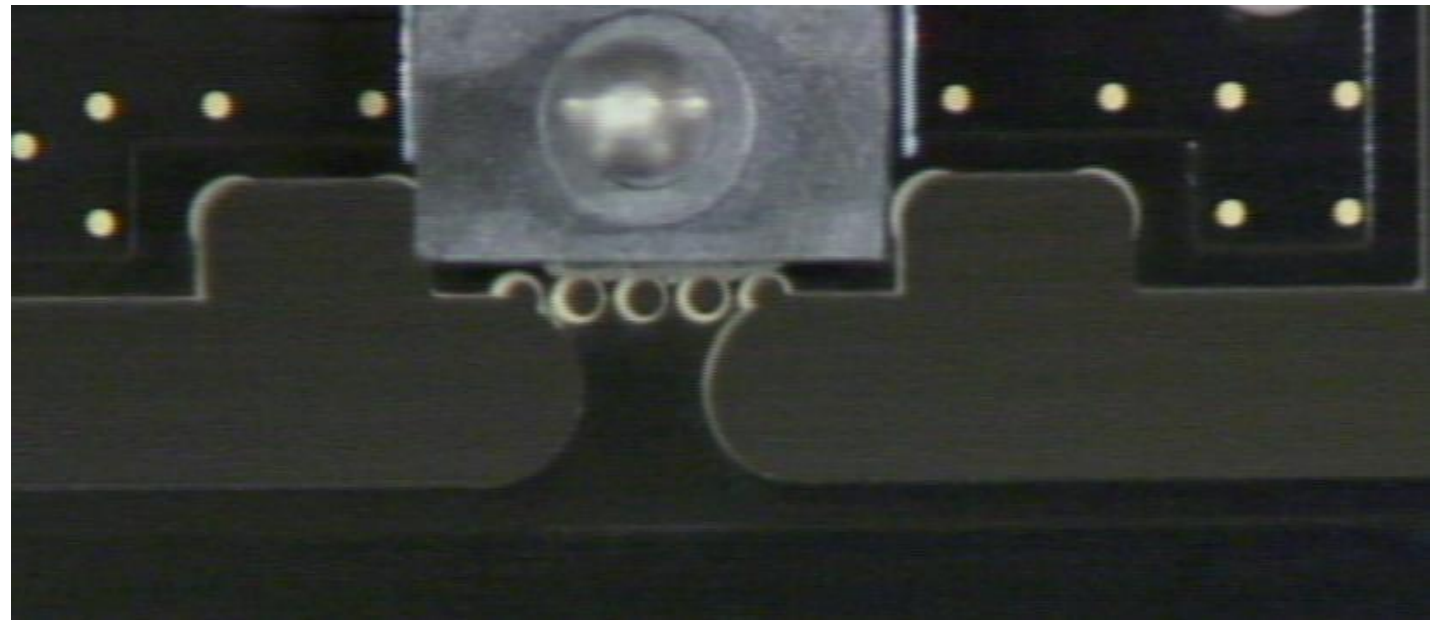
The hole in the guide pins was little to small, which resulted in that 2 connectors got broken during assembly.



# Eksempler fra DFM og NPI

## Plassering av tabs

- Minimum avstand fra kopper til kontur/tab 0,4mm + minimum isolasjonsavstand, foretrukket 1,5mm
- Spesifiser på komponentplasseringstegning maks utstikk av tab rester utover kontur
- Plasser taber i åpne områder men med passelige avstander mellom tabs og til hjørner (IPC-7351)



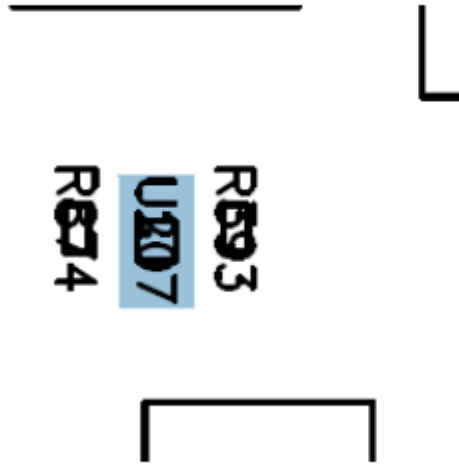


# Eksempler fra DFM og NPI

## Overflødig silketrykk

- Begrens silketrykk til nødvendig og ønskelig informasjon
- Silketrykk nær loddepader kan redusere kvalitet på pastatrykk og dekning på AOI

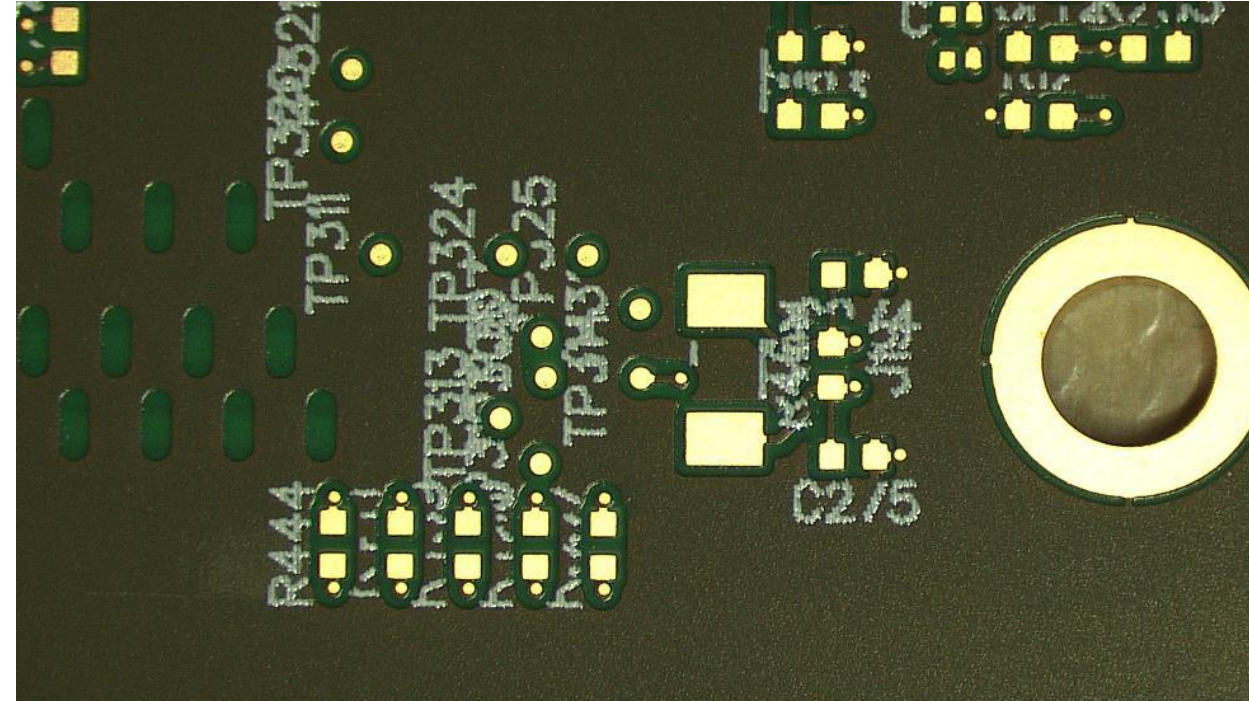
During preparation it was not detected that there where orientation on pos U207 since reference name was placed over the shape.



Before zoom



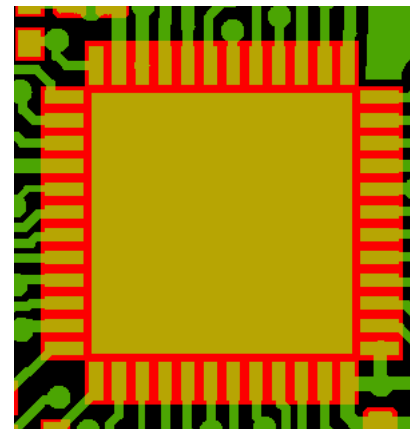
After zoom



# Eksempler fra DFM og NPI

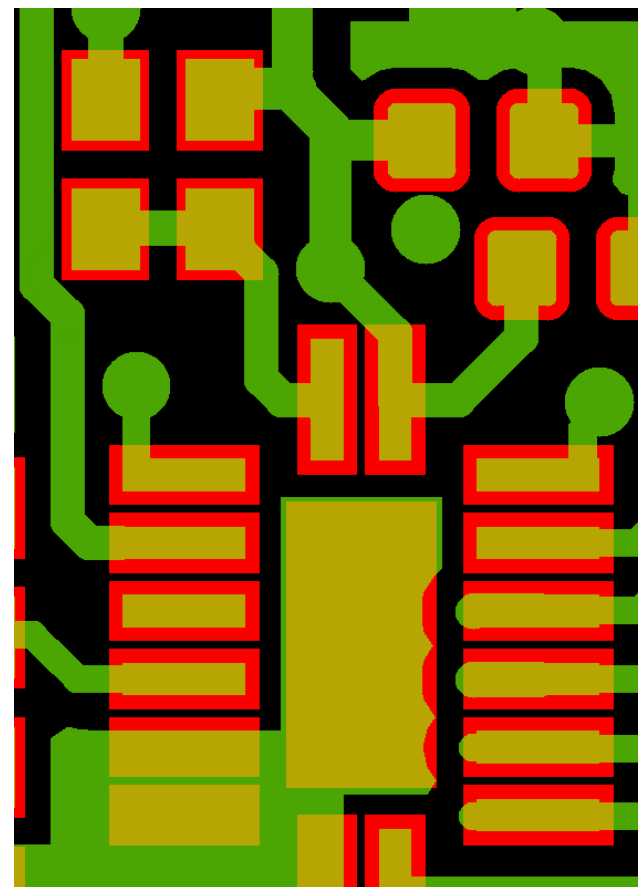
Manglende loddemaske mellom pader (solder dam)

- Ha riktig loddemaske klaring i forhold til komponent type
- Hold min 100um solder mask web bredde
- For kort med fine pitch komponenter unngå andre farger på loddemaske enn standard grønn, spesielt ved web bredder mindre enn 150um.



### 3.3.1 Solder resist features to ensure no encroachment

| FEATURE TYPE             | POSITION | ≤ 35 um                |  | ≤ 70 um |  | ≤ 105 um   |  |
|--------------------------|----------|------------------------|--|---------|--|------------|--|
|                          |          |                        |  |         |  |            |  |
| SMT TO COVERED COPPER    | A        | 100 um                 |  | 150 um  |  | 250 um     |  |
| COPPER TO COPPER SPACING | B        | 150 um                 |  | 200 um  |  | 300 um     |  |
| SOLDER MASK OVERSIZE     | C        | 25 um                  |  | 50 um   |  | 50 um      |  |
| MINIMUM SOLDERMASK WEB   | D        | Green solder mask      |  |         |  | min 70 um  |  |
|                          |          | White solder mask      |  |         |  | min 150 um |  |
|                          |          | Blue solder mask       |  |         |  | min 135 um |  |
|                          |          | Black solder mask      |  |         |  | min 135 um |  |
|                          |          | Red Solder mask        |  |         |  | min 100 um |  |
|                          |          | Green Flex solder mask |  |         |  | min 100 um |  |

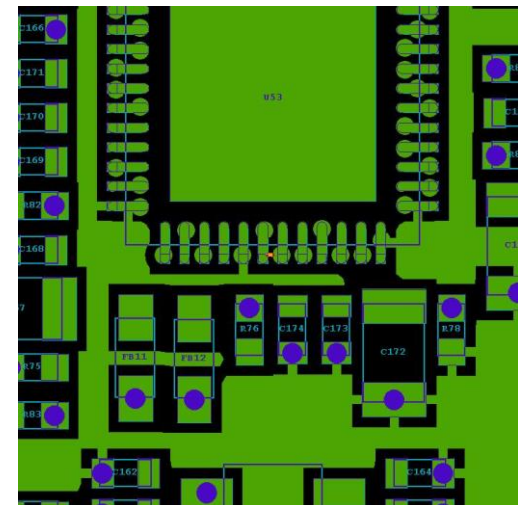
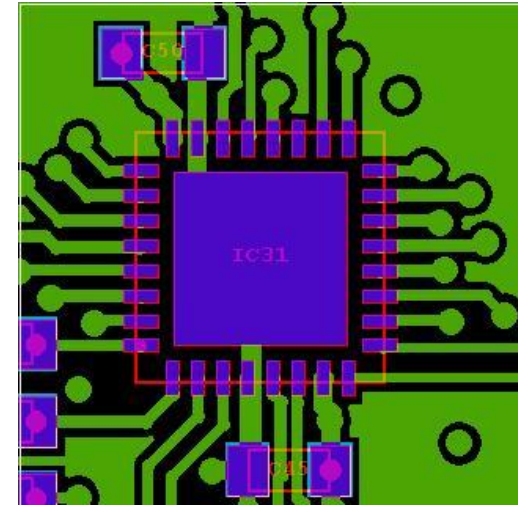
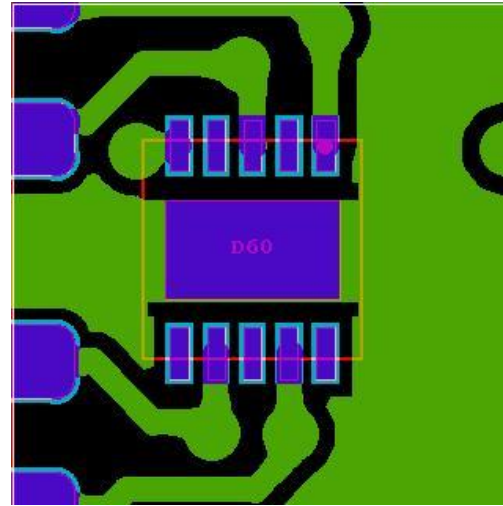
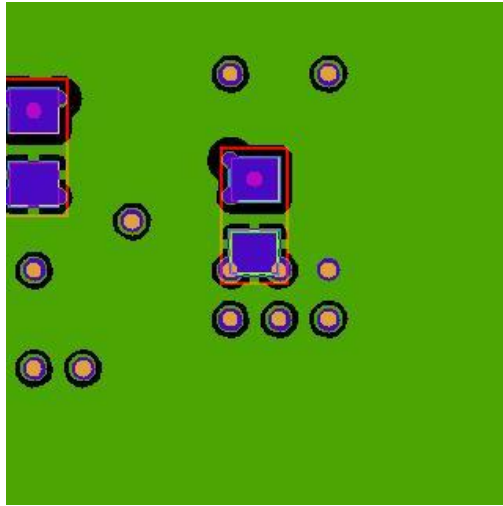
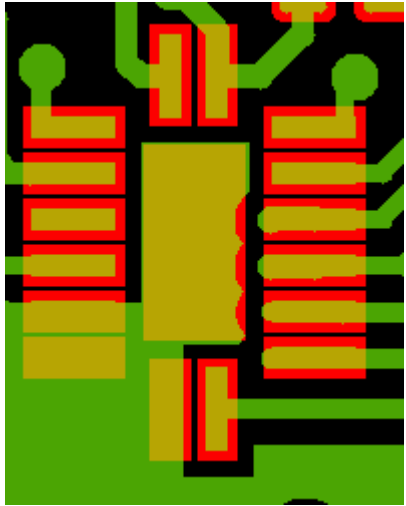


(Fra Hitech's website)

# Eksempler fra DFM og NPI

## Pad definisjon

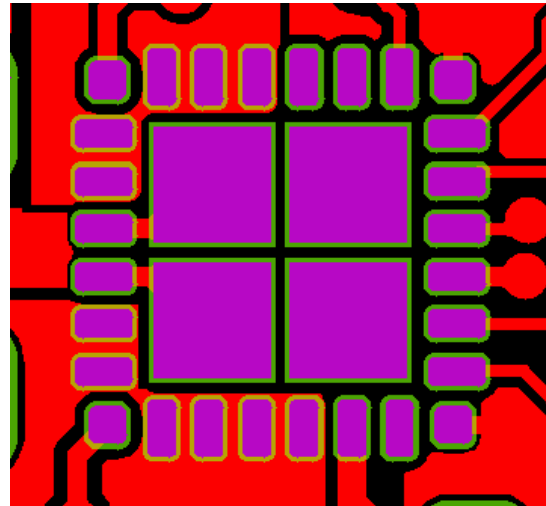
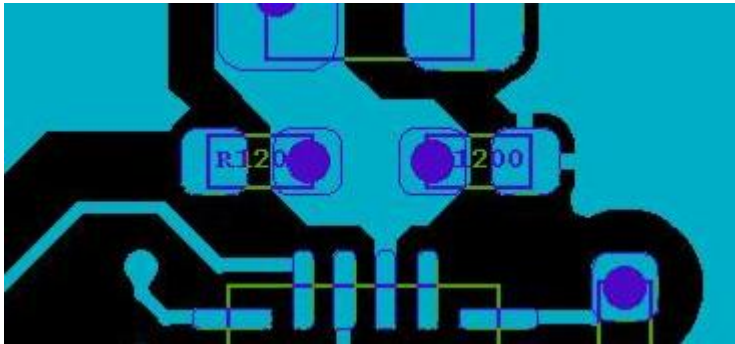
- Pader definert av andre features eller attributer



# Eksempler fra DFM og NPI

## Pad definisjon

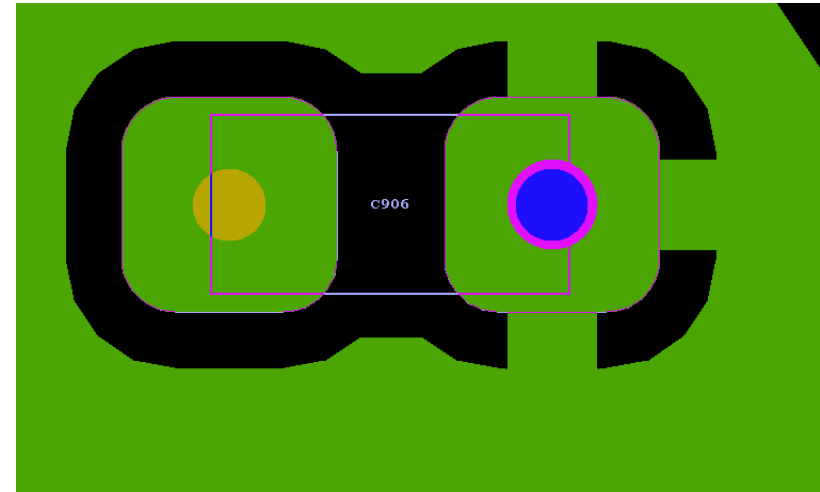
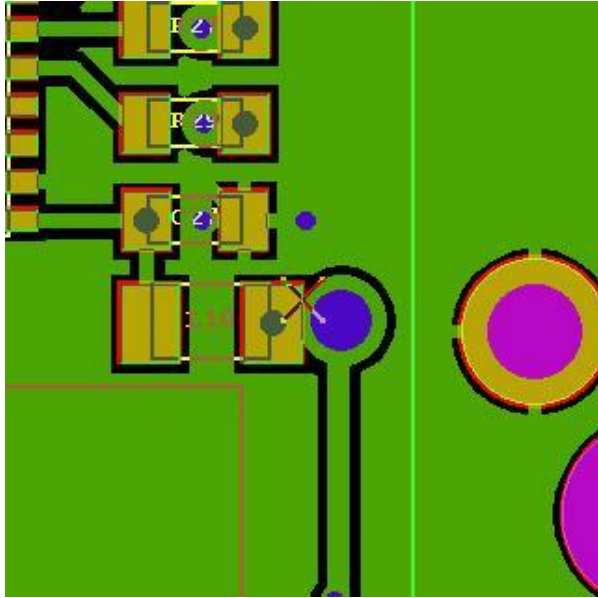
- Pader definert av loddemaskeklaring kan prosentmessig bli ganske mye større, påvirker pastamengde og termisk balanse
- Kitron rapporterer generelt ikke termisk ubalanse mellom pader på chip komponenter da dette ikke er noe stort problem slik vi kjører vår prosess men dette kan ha større betydning ved andre produksjonsprosesser, volumer eller legeringer



# Eksempler fra DFM og NPI

## Vias i pad (mekanisk boret)

- Alvorlighetsgrad er avhengig av via type, komponent type, bredde på annular ring og om hullet sitter i eller utenfor pad
- Kan mitigeres ved plugging og overplettering men dette koster

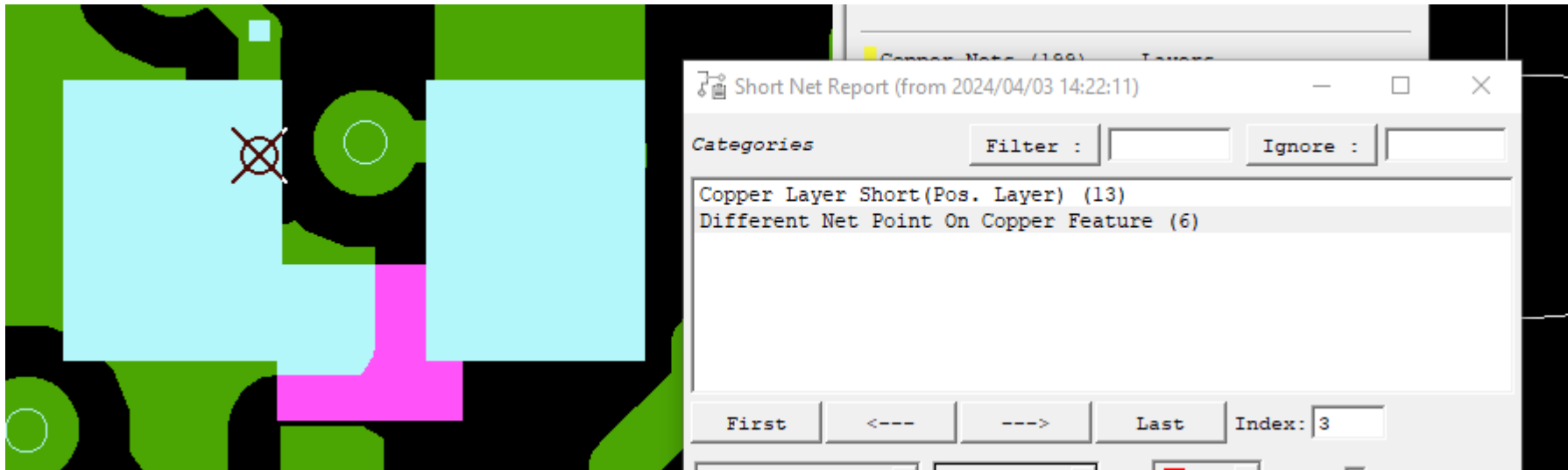
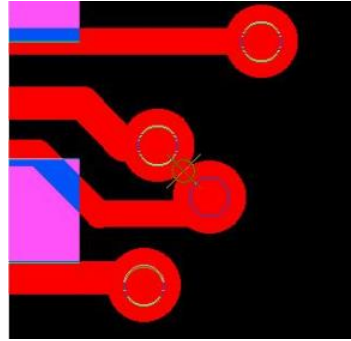


# Eksempler fra DFM og NPI

## Nettlistefeil

- De aller fleste feil som detekteres er falske flagg av forskjellige grunner men det som er reelt er ofte fatale feil

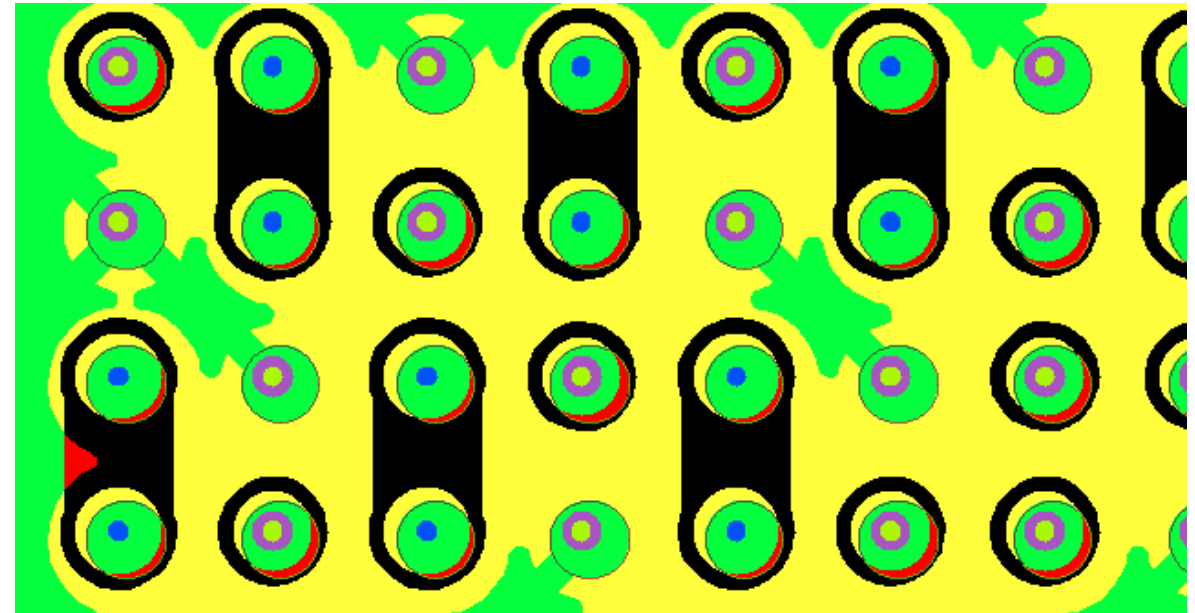
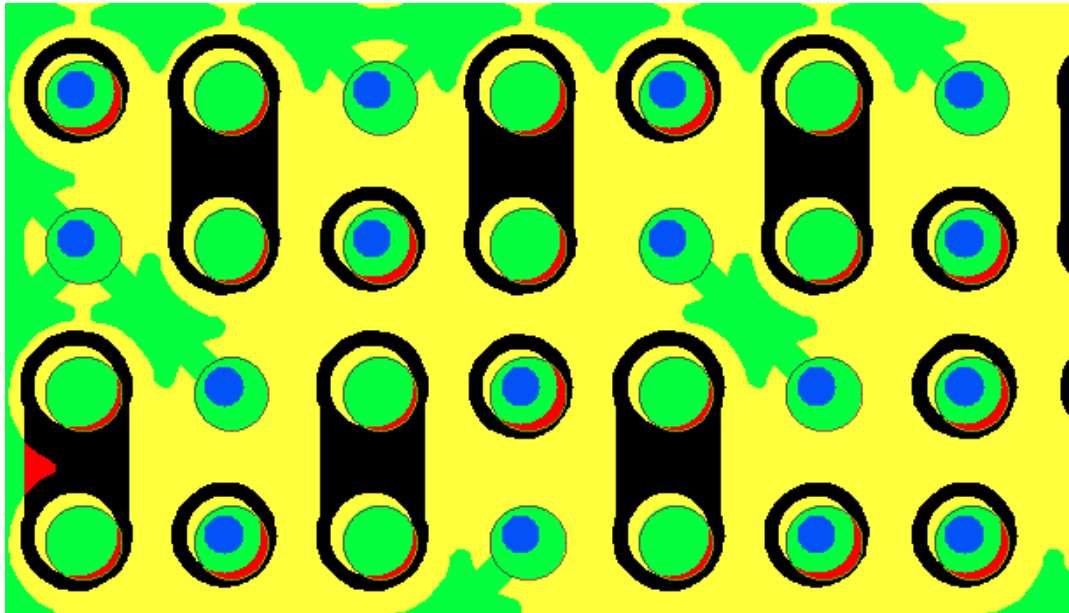
|   |  |        |          |
|---|--|--------|----------|
| 1 | Too close features # 5492 (Net RL1_TEMP) and # 5491 (Net RL2_TEMP): 0.272146 mils (6.912500 mic) | opened | critical |
|---|--|--------|----------|



# Eksempler fra DFM og NPI

## Feil via plassering (BGA fanout)

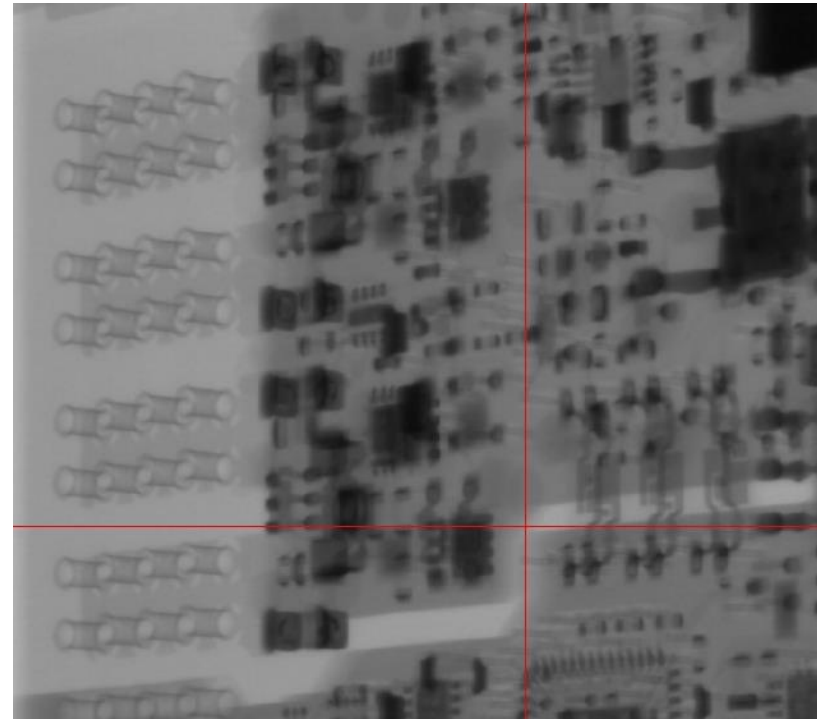
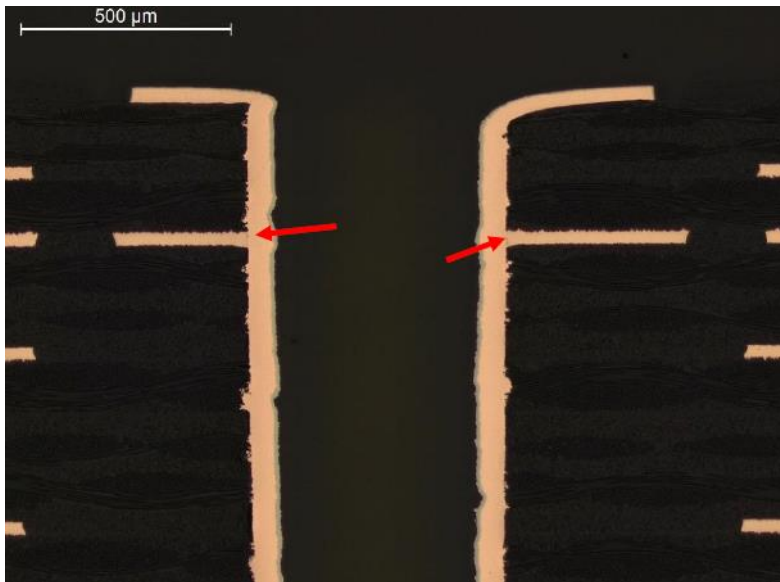
- Laser via plassert oppå en cap plettering, kan oppstå sirkulært brudd
- Blindt eller gjennomgående (Type VII) mekanisk boret via i BGA pad, kan forårsake mekanisk kraft og brudd i lodding/intermetallisk sjikt



# Eksempler fra DFM og NPI

Fjerning av ikke funksjonelle pader på hull for lodding (komponenthull) og copper pour i isolerte områder

- Kan forårsake lamineringsproblemer og delaminering under lodding
- Kan forårsake pålitelighetsproblemer (vakkel/brudd)
- Bør begrenses til via hull

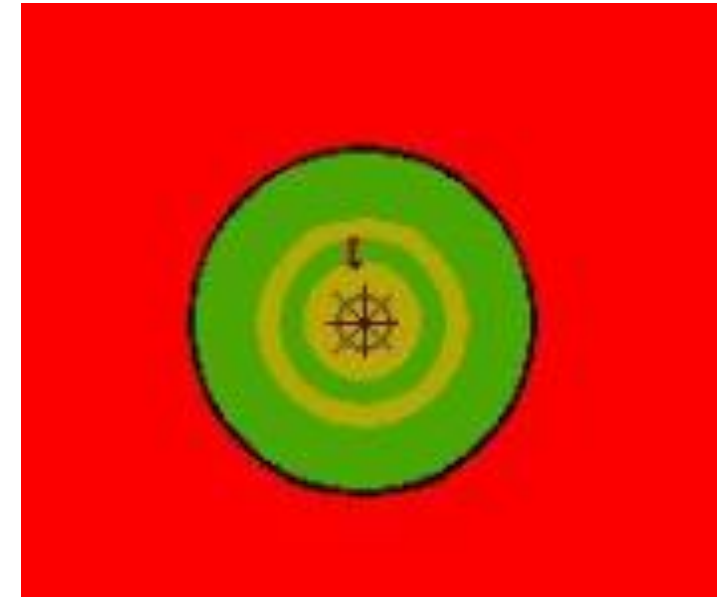
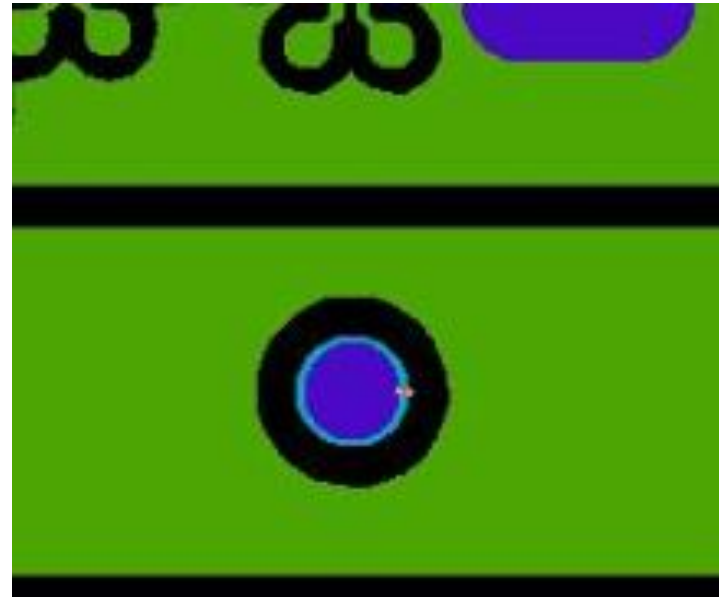
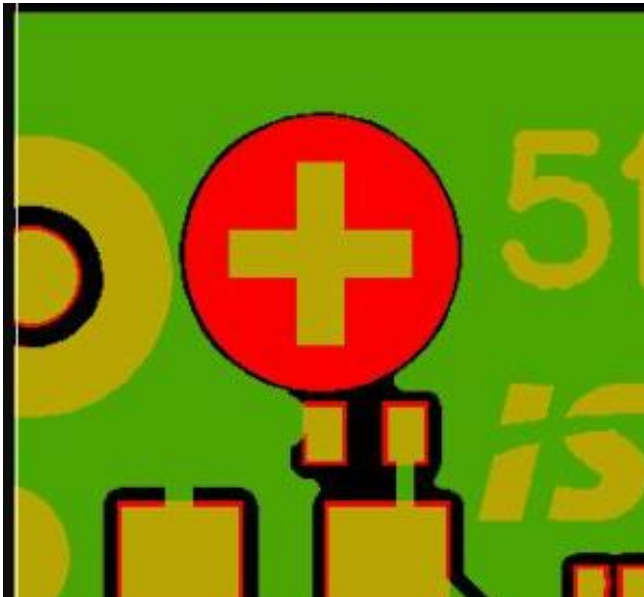
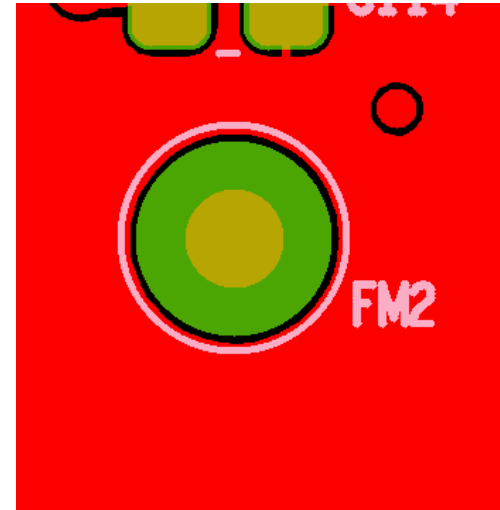




# Eksempler fra DFM og NPI

## Fiducialmerker

- Min 1mm med 2mm åpning i loddemaske (1,5/3mm for HASL)
- Trekk tilbake kopper litt mer enn loddemaske
- Min 2 globale, diagonal, component fiducials brukes ikke

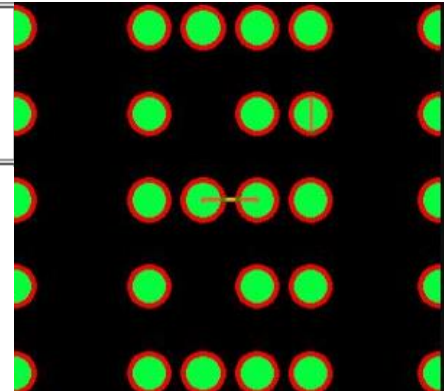


# Eksempler fra DFM og NPI

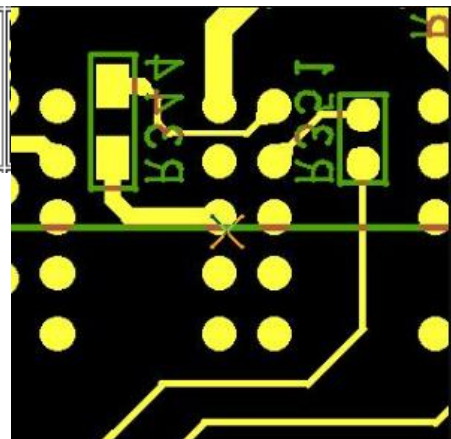
## Testpunkter

- Min diameter 1mm
- Min afstand fra component pad 1mm
- Min pitch 1,27mm (1,9mm anbefalt)

|   |                            |        |  |      |          |      |  |
|---|----------------------------|--------|--|------|----------|------|--|
| 3 | chk:Testpoint to testpoint | opened |  | warm | 1.270000 | 7000 | 15/03/22 grug: Recommended minimum 1,9mm |
|---|----------------------------|--------|--|------|----------|------|--|

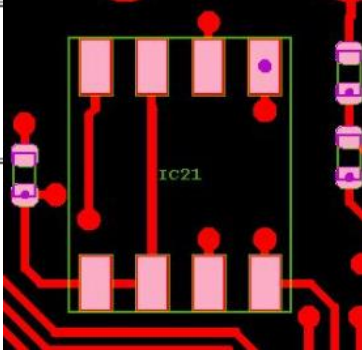


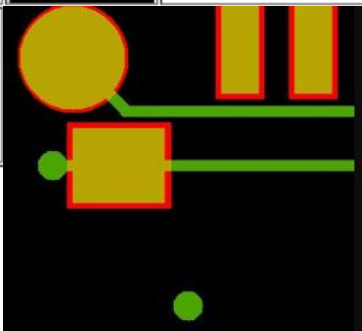
|   |                     |        |  |     |          |     |  |
|---|---------------------|--------|--|-----|----------|-----|--|
| 6 | chk:Testpoint to SS | opened |  | hot | 0.000000 | 300 |  |
|---|---------------------|--------|--|-----|----------|-----|--|



# Eksempler fra DFM og NPI

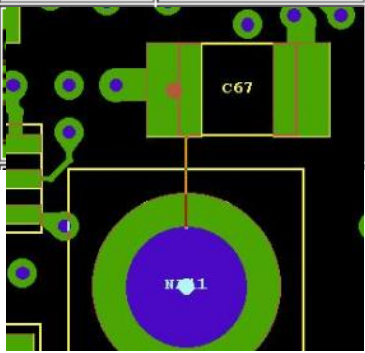
## Diverse

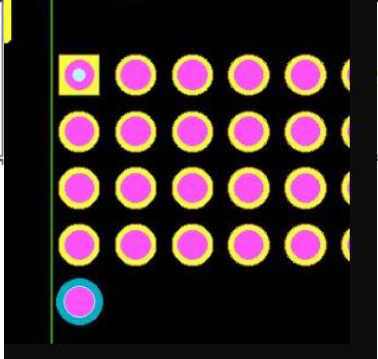
|   |                                    |        |      |   |           |  |
|---|------------------------------------|--------|------|---|-----------|--|
| 7 | Solder paste data not 1:1 with pad | opened | warm |  | 40.204755 |  |
|---|------------------------------------|--------|------|---|-----------|--|

|   |   |        |      |   |           |  |
|---|---|--------|------|---|-----------|--|
| 9 | Solder mask clearance is too large vs spacing | opened | warm |  | 10.672812 | 20/03/23 grug: Change solder mask clearance to 50um glob |
|---|---|--------|------|---|-----------|--|

# Eksempler fra DFM og NPI

## Diverse

|    |  |        |  |      |          |   |            |
|----|--|--------|--|------|----------|---|------------|
| 11 | chk: Toeprint to Mounting Hole (Primary) | opened |  | warm | 2.438400 |  | 127.431800 |
|----|--|--------|--|------|----------|---|------------|

|    |  |        |  |      |  |  |          |
|----|--|--------|--|------|--|--|----------|
| 16 | Square THD pads (may promote bridging) | opened |  | warm |  |  | 9.869460 |
|----|--|--------|--|------|--|--|----------|



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